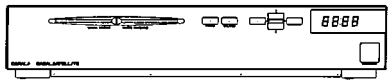
Service Manual



ORDER NO.
ARP3079

CANAL PLUS TUNER

TS5
BCT-1510
BCT-1520
BCT-1530

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model				Power Requirement	Remarks
	TS5	BCT-1510	BCT-1520	BCT-1530		
NYXK/FR	◯	–	–	–	AC230V	
NYXK/FR1	◯	–	–	–	AC230V	
NYXK/FR2	◯	–	–	–	AC230V	
NYXK/FR3	◯	–	–	–	AC230V	
NYXK/SP	–	◯	–	–	AC230V	
NYXK/IT	–	–	◯	–	AC230V	
NYWXKPL	–	–	–	◯	AC230V	

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians ; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 – Proposition 65

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

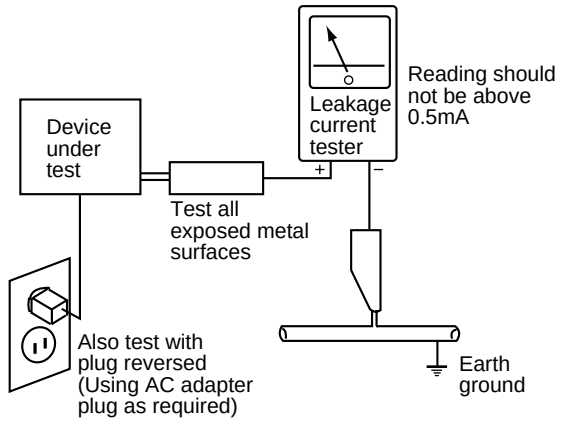
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.


Reading should not be above 0.5mA
Leakage current tester
+
–
Device under test
Test all exposed metal surfaces
Also test with plug reversed (Using AC adapter plug as required)
Earth ground

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

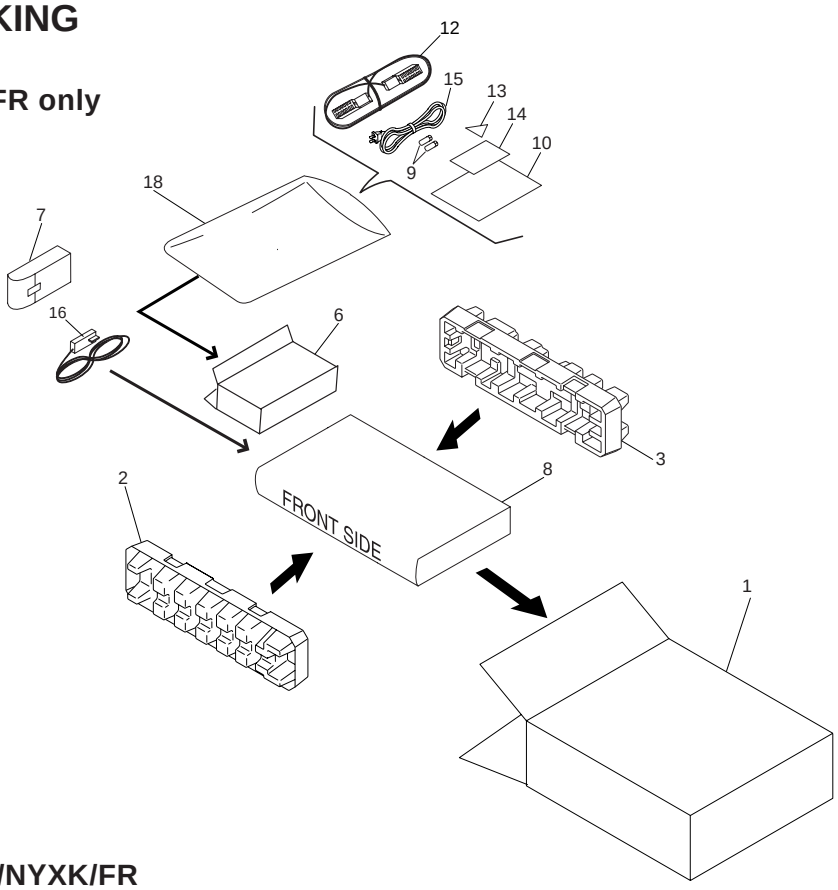
TS5, BCT-1510, BCT-1520, BCT-1530

2. EXPLODED VIEWS AND PARTS LIST

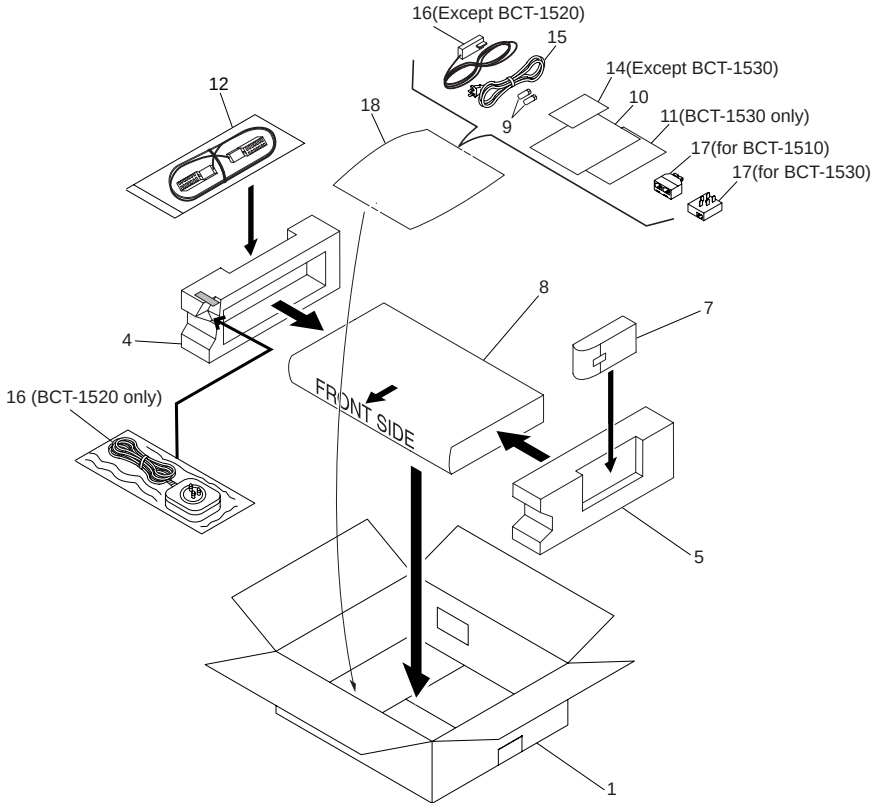
NOTES: ●*Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
●*The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
●*Screws adjacent to ▼ mark on the product are used for disassembly.*

2.1 PACKING

TS5/NYXK/FR only



Except TS5/NYXK/FR



(1) PACKING PARTS LIST

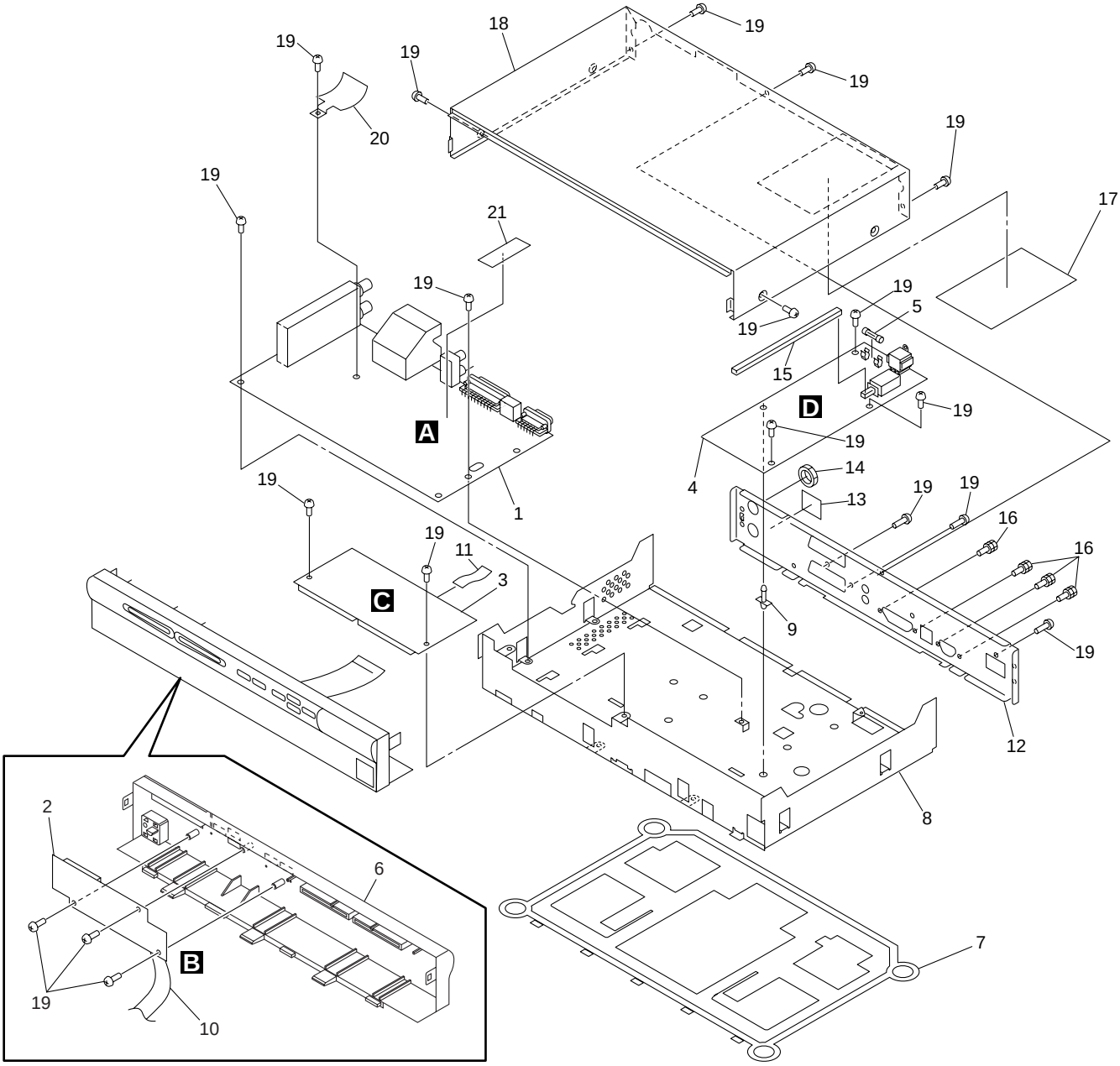
Mark	No.	Description	Part No.
	1	Packing Case	See Contrast Table(2)
	2	Pulp Mold Pad F	See Contrast Table(2)
	3	Pulp Mold Pad R	See Contrast Table(2)
	4	Side Pad L	See Contrast Table(2)
	5	Side Pad R	See Contrast Table(2)
	6	Sub Packing Case	See Contrast Table(2)
	7	Remote Control Unit	See Contrast Table(2)
	8	Sheet	AHG1153
	9	Battery (R03) 2P	VEM1018
	10	Instruction Manual	See Contrast Table(2)
	11	Instruction Manual 2	See Contrast Table(2)
	12	Scart Cable(1m:Black)	See Contrast Table(2)
NSP	13	Sticker	See Contrast Table(2)
NSP	14	Modem Approval Sheet	See Contrast Table(2)
⚠	15	AC Power Cord (2m:Black)	BDG1035
	16	Modem Cable (10m:White)	See Contrast Table(2)
NSP	17	Modem Adapter	See Contrast Table(2)
NSP	18	Catalogue Bag	BHG1047

(2) CONTRAST TABLE

TS5/NYXK/FR, TS5/NYXK/FR1, TS5/NYXK/FR2, TS5/NYXK/FR3, BCT-1510/NYXK/SP, BCT-1520/NYXK/IT and BCT-1530/NYWXKPL are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.							Remarks
			TS5 /NYXK/FR	TS5 /NYXK/FR1	TS5 /NYXK/FR2	TS5 /NYXK/FR3	BCT-1510 /NYXK/SP	BCT-1520 /NYXK/IT	BCT-1530 /NYWXKPL	
	1	Packing Case	BHD1489	BHD1369	BHD1369	BHD1369	BHD1375	BHD1480	BHD1442	
	2	Pulp Mold Pad F	BHX1028	Not used	Not used	Not used	Not used	Not used	Not used	
	3	Pulp Mold Pad R	BHX1029	Not used	Not used	Not used	Not used	Not used	Not used	
	4	Side Pad L	Not used	BHA1146	BHA1146	BHA1146	BHA1146	BHA1146	BHA1146	
	5	Side Pad R	Not used	BHA1147	BHA1147	BHA1147	BHA1147	BHA1147	BHA1147	
	6	Sub Packing Case	BHB1036	Not used	Not used	Not used	Not used	Not used	Not used	
	7	Remote Control Unit	BXD1010	BXD1010	BXD1010	BXD1010	BXD1016	BXD1018	BXD1037	
	10	Instruction Manual (French)	BRC1030	BRC1021	BRC1022	BRC1026	Not used	Not used	Not used	
	10	Instruction Manual (Spanish)	Not used	Not used	Not used	Not used	BRC1004	Not used	Not used	
	10	Instruction Manual (Italian)	Not used	Not used	Not used	Not used	Not used	BRC1027	Not used	
	10	Instruction Manual (Polish)	Not used	Not used	Not used	Not used	Not used	Not used	BRC1011	
	11	Instruction Manual 2 (Polish)	Not used	Not used	Not used	Not used	Not used	Not used	BRC1012	
	12	Scart Cable	BDH1018	BDH1027	BDH1027	BDH1027	BDH1018	BDH1018	BDH1018	
NSP	13	Sticker	BAX1271	Not used	Not used	Not used	Not used	Not used	Not used	
NSP	14	Modem Approval Sheet	BRM1034	BRM1034	BRM1034	BRM1034	BRM1035	BRM1036	Not used	
	16	Modem Cable	BDH1014	BDH1014	BDH1014	BDH1014	BDH1015	BDH1016	BDH1015	
NSP	17	Modem Adapter	Not used	Not used	Not used	Not used	BKP1124	Not used	BKP1130	

2.2 EXTERIOR SECTION



(1) EXTERIOR SECTION PARTS LIST

Mark	No.	Description	Part No.
	1	MAIN ASSY(FRANCE)	See Contrast Table (2)
	2	FRONT ASSY	BWE1102
	3	CARD ASSY	BWE1080
⚠	4	POWER ASSY	BXF1139
⚠	5	Fuse (0109: T2.5AH250V)	REK1102
	6	Front Panel Assy	See Contrast Table (2)
	7	Plastic Base	BMA1002
	8	Chassis	BNA1151
	9	PCB Support	AEC1215
	10	21P FFC(J1)	BDD1042
	11	12P FFC(J2)	BDD1022
	12	Rear Panel Assy	See Contrast Table (2)
NSP	13	Name Label	See Contrast Table (2)
	14	Washer Faced Nut	BBN1005
	15	Joint	BMR1133
	16	Hexagon Headed screw	BBA1059
	17	Barrier	BEC1231
	18	Bonnet Case	See Contrast Table (2)
	19	Screw	BBZ30P080FZK
	20	Heat Sink	BNH1049
	21	Serial No. Label	See Contrast Table (2)

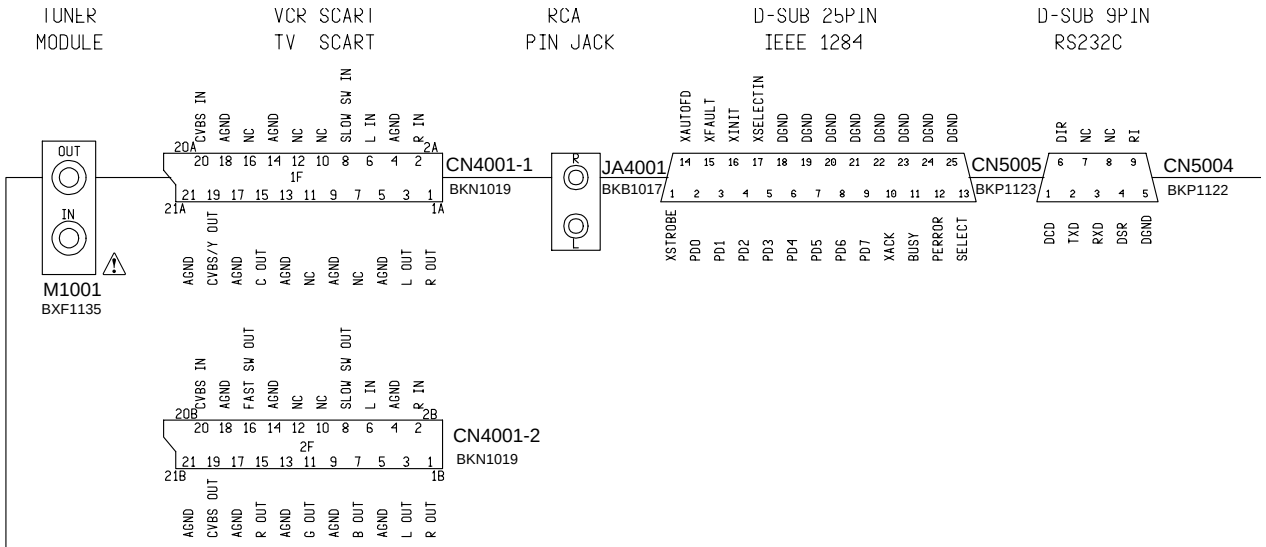
(2) CONTRAST TABLE

TS5/NYXK/FR, TS5/NYXK/FR1, TS5/NYXK/FR2, TS5/NYXK/FR3, BCT-1510/NYXK/SP, BCT-1520/NYXK/IT and BCT-1530/NYWXKPL are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.							Remarks
			TS5 /NYXK/FR	TS5 /NYXK/FR1	TS5 /NYXK/FR2	TS5 /NYXK/FR3	BCT-1510 /NYXK/SP	BCT-1520 /NYXK/IT	BCT-1530 /NYWXKPL	
	1	MAIN ASSY	BWE1103	BWE1103	BWE1103	BWE1103	BWE1115	BWE1115	BWE1110	
	6	Front Panel Assy	BWX1144	BWX1144	BWX1144	BWX1144	BWX1145	BWX1191	BWX1146	
	12	Rear Panel Assy	BWX1168	BWX1168	BWX1168	BWX1168	BWX1169	BWX1170	BWX1171	
NSP	13	Name Label	BAL1400	BAL1414	BAL1415	BAL1416	BAL1401	BAL1402	BAL1403	
	18	Bonnet Case	BNE1120	BNE1120	BNE1120	BNE1120	BNE1120	BNE1122	BNE1120	
	21	Serial No. Label	BAX1145	BAX1145	BAX1145	BAX1145	BAX1181	BAX1189	BAX1250	

3. SCHEMATIC DIAGRAM

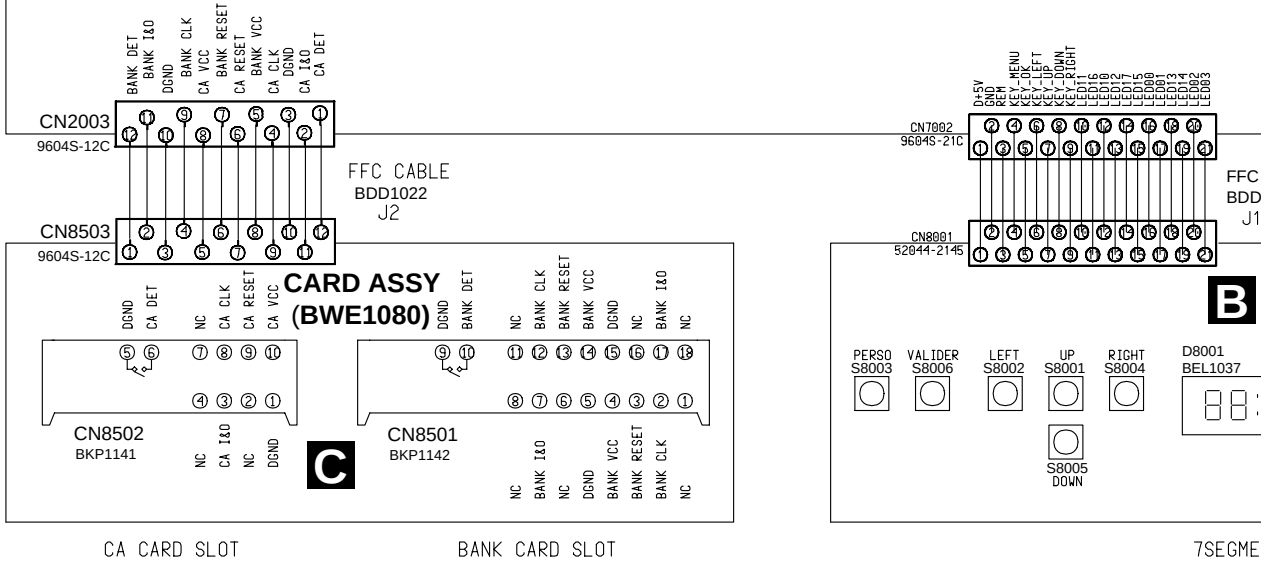
3.1 OVERALL WIRING DIAGRAM



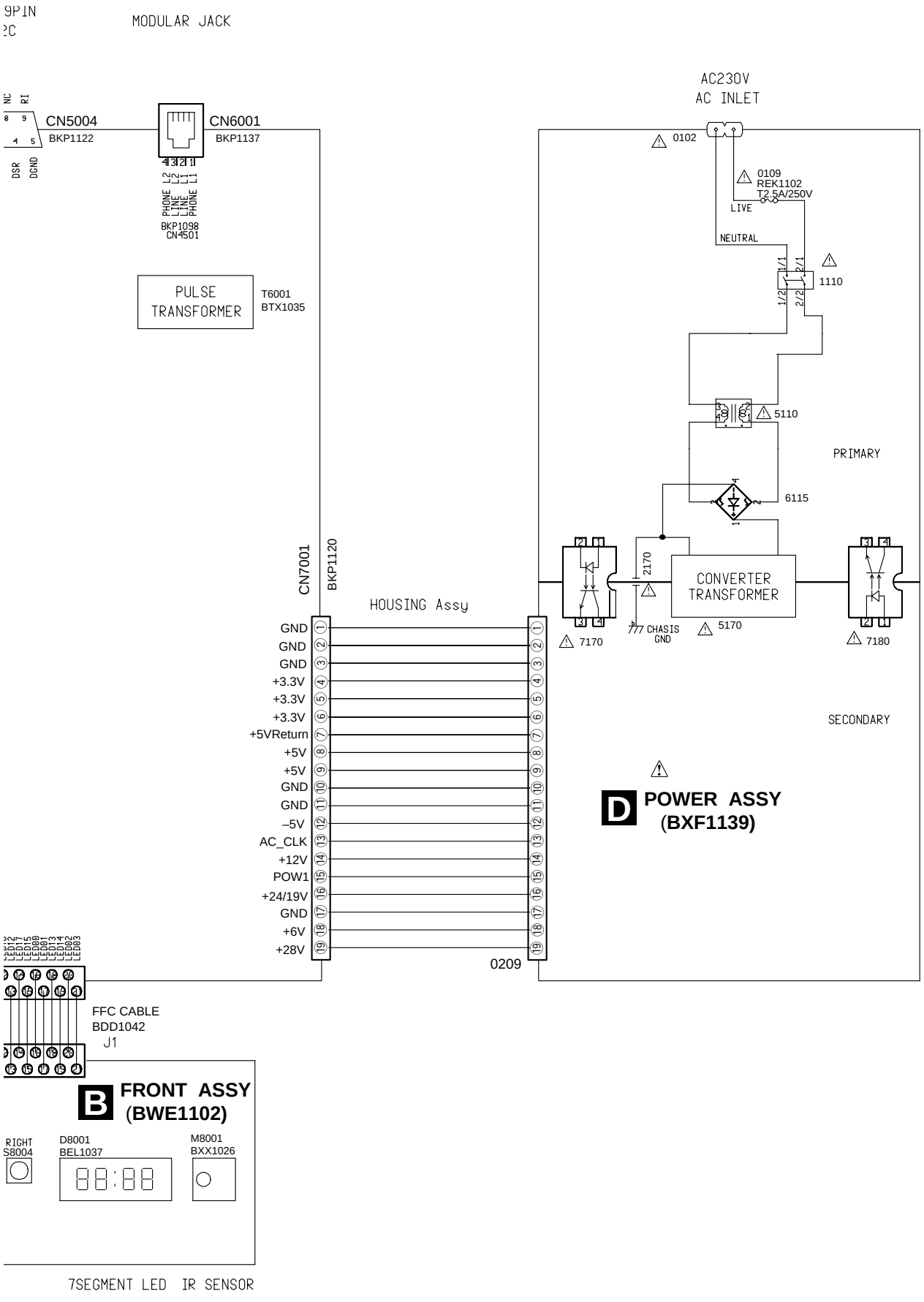
A (A1/7-A7/7) MAIN ASSY

(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)

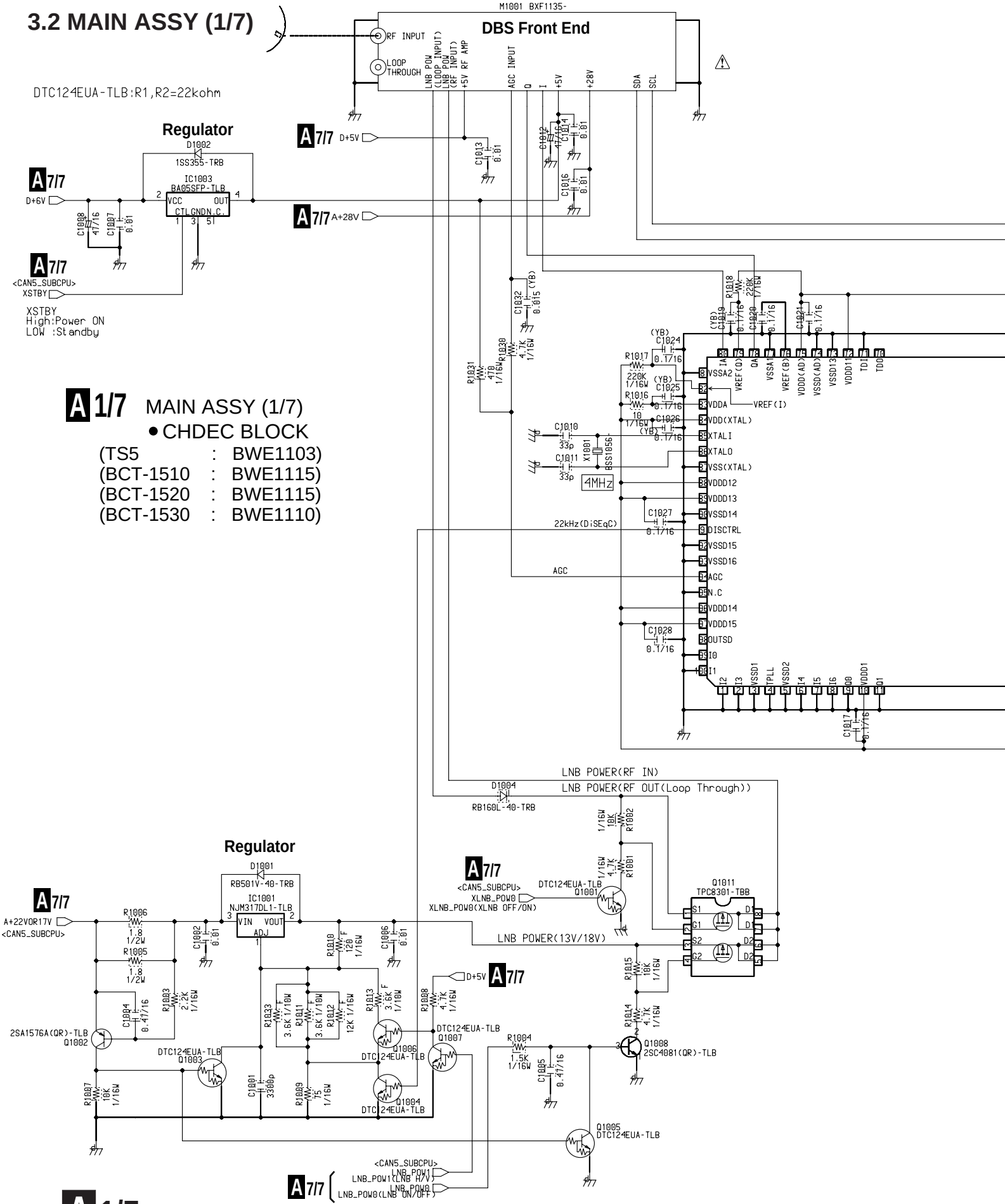
CHDEC BLOCK	:	B1E1103
DMXCPU BLOCK	:	B2E1103
MEMORY BLOCK	:	B3E1103
ANALOG AV BLOCK	:	B4E1103
IO BLOCK	:	B5E1103
MODEM BLOCK	:	B6E1103
SUBPOWER BLOCK	:	B7E1103

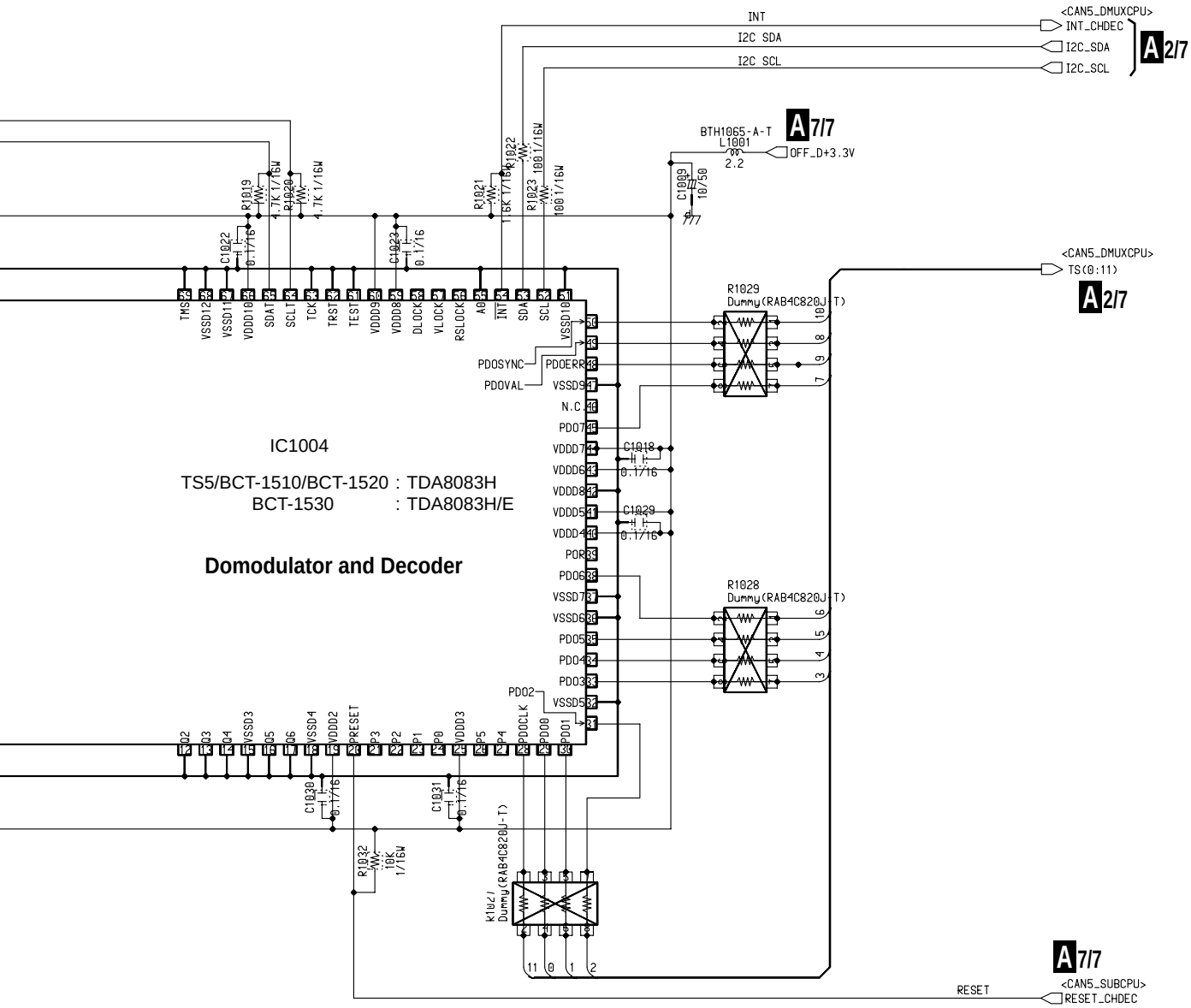


Note : When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".



TS5, BCT-1510, BCT-1520, BCT-1530
3.2 MAIN ASSY (1/7)





LNB_POW0 { Low: LNB OFF(External)
High: LNB ON (Internal)

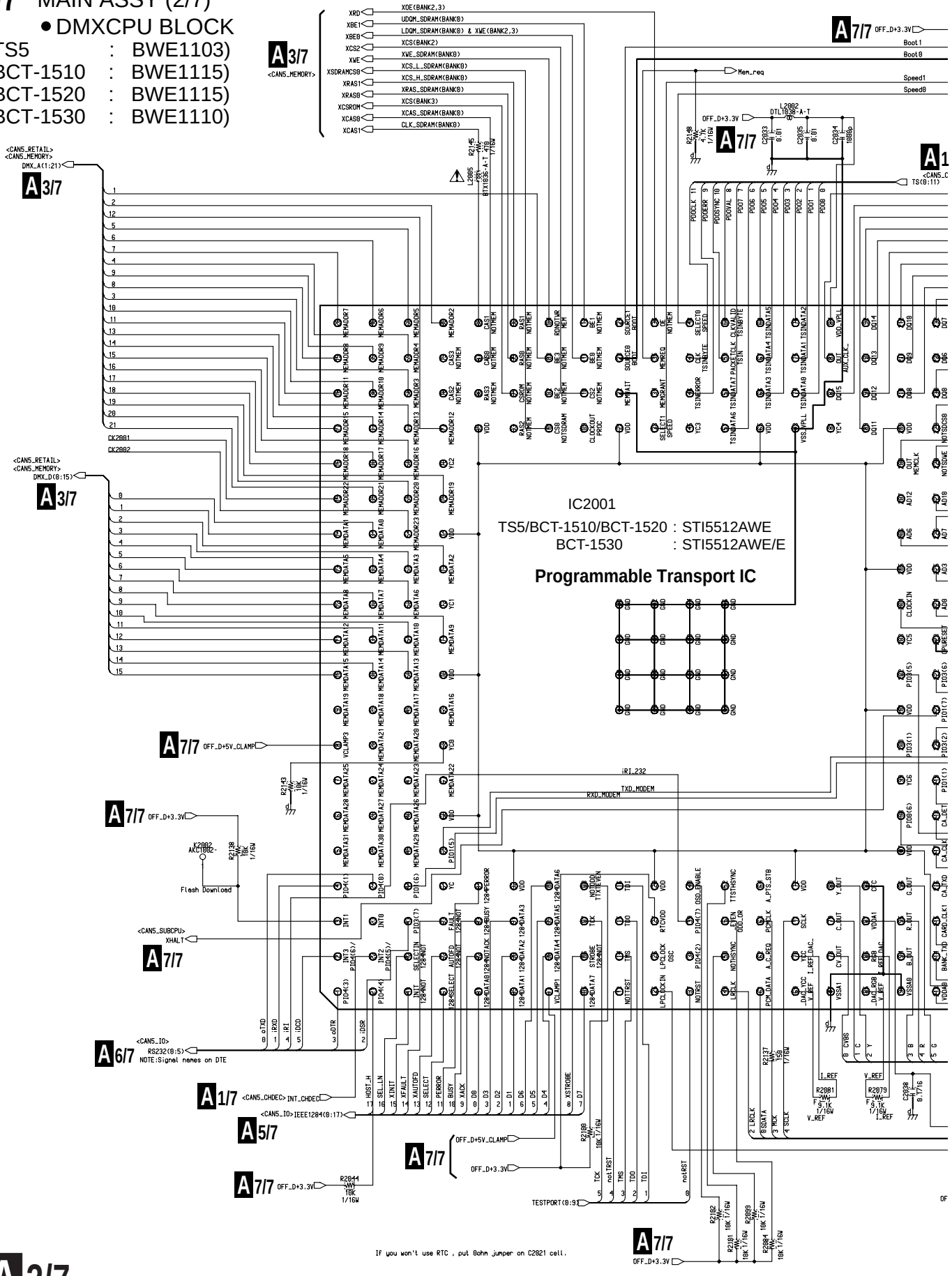
LNB_POW1 { Low: LNB V(13V)
High: LNB H(18V)

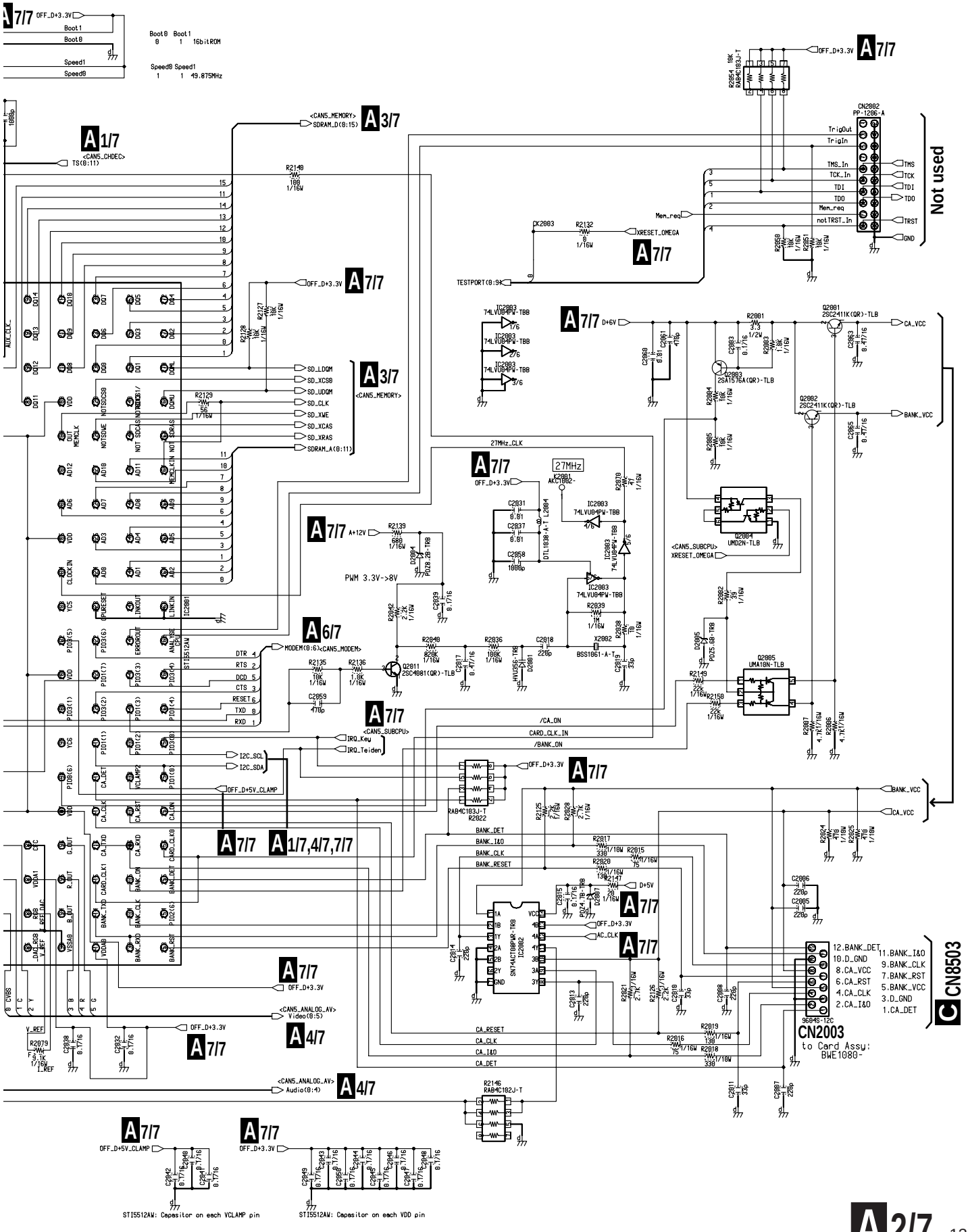
TS5, BCT-1510, BCT-1520, BCT-1530
3.3 MAIN ASSY (2/7)

A 2/7 MAIN ASSY (2/7)

- DMXCPU BLOCK

(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)

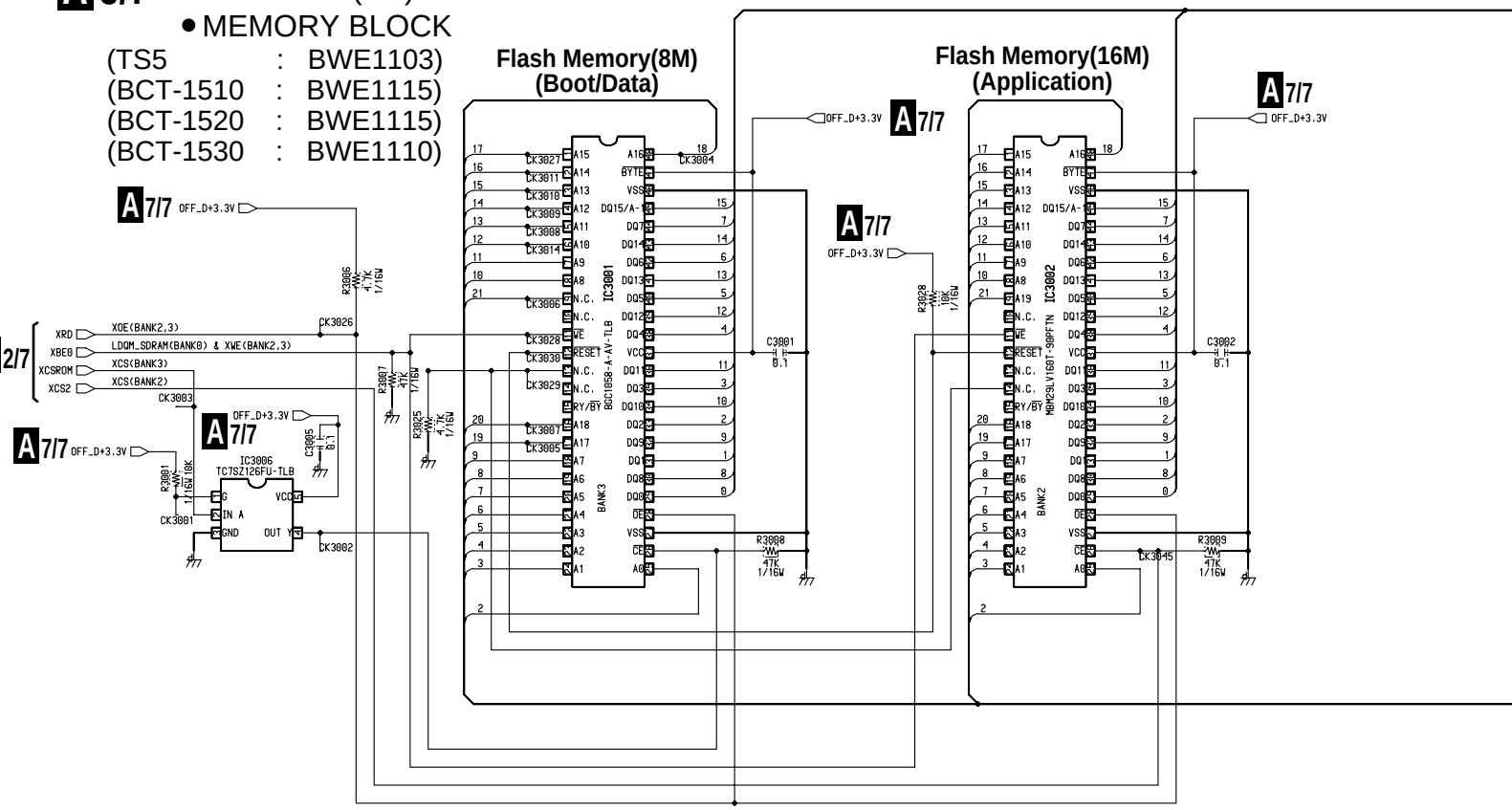

IC2001
TS5/BCT-1510/BCT-1520 : STI5512AWE
BCT-1530 : STI5512AWE/E
Programmable Transport IC
Flash Download
If you won't use RTC , put 0ohm jumper on C2021 cell.

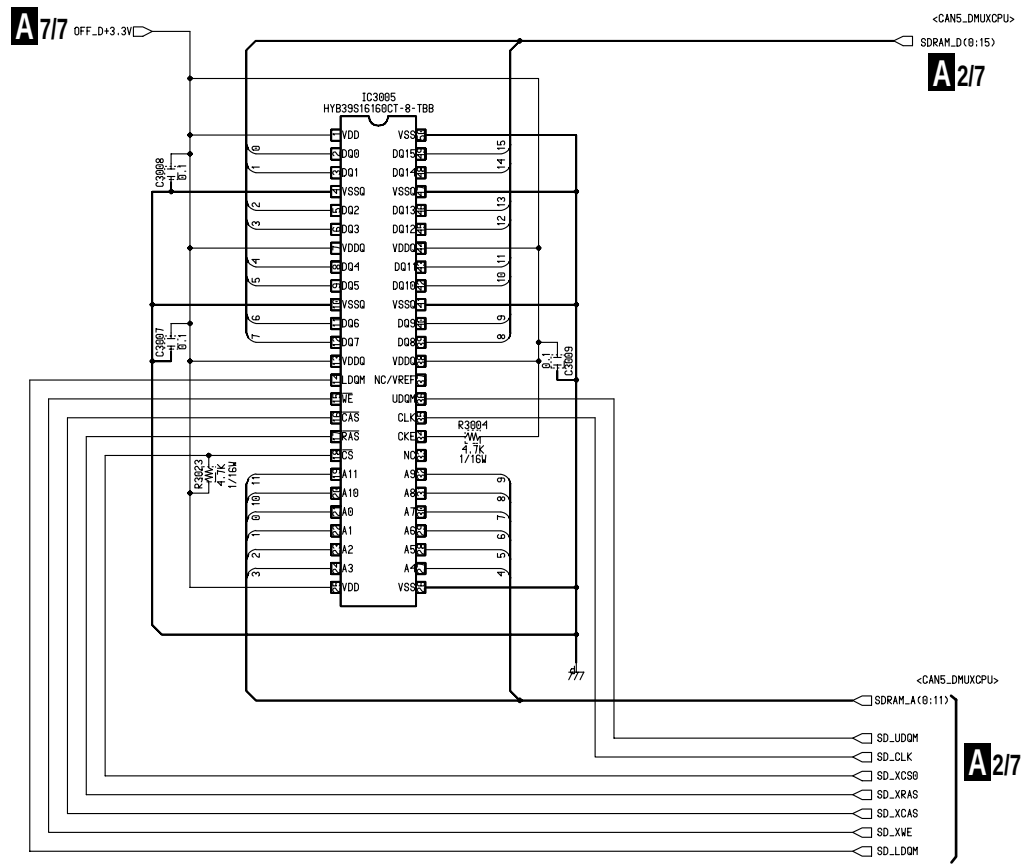

Not used
CN2003
to Card Assy:
BWE1080-
CN8503
STI5512AW: Capasitor on each VCLAMP pin
STI5512AW: Capasitor on each VDD pin

A 3/7 MAIN ASSY (3/7)

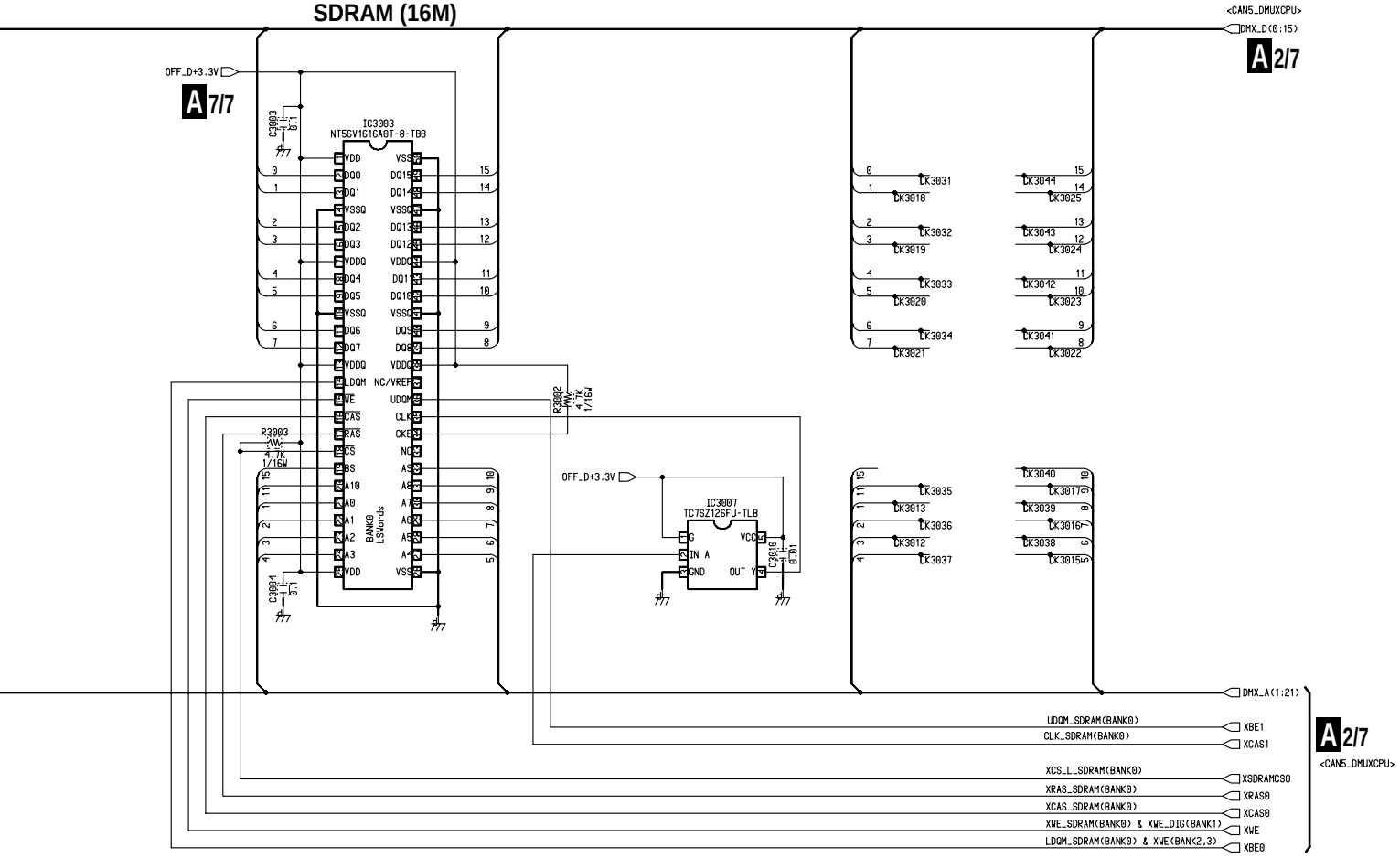
- MEMORY BLOCK

(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)





SDRAM (16M)


OFF_D+3.3V
A7/7
IC3003
NT56V1616A0T-8-TBB
BANK0
LSWords
R3003
4.7K
1/16W
R3002
4.7K
1/16W
IC3007
TC7SZ126FU-TLB
CK3031
CK3018
CK3032
CK3019
CK3033
CK3020
CK3034
CK3021
CK3044
CK3025
CK3043
CK3024
CK3042
CK3023
CK3041
CK3022
CK3035
CK3013
CK3036
CK3012
CK3037
CK3040
CK3017
CK3039
CK3016
CK3038
CK3015
<CAN5_DMUXCPU>
DMX_D(0:15)
A2/7
DMX_A(1:21)
UDQM_SDRAM(BANK0)
CLK_SDRAM(BANK0)
XBE1
XCAS1
XCS_L_SDRAM(BANK0)
XRAS_SDRAM(BANK0)
XCAS_SDRAM(BANK0)
XWE_SDRAM(BANK0) & XWE_DIG(BANK1)
LDQM_SDRAM(BANK0) & XWE(BANK2,3)
XSDRAMCS0
XRAS0
XCAS0
XWE
XBE0
A2/7
<CAN5_DMUXCPU>

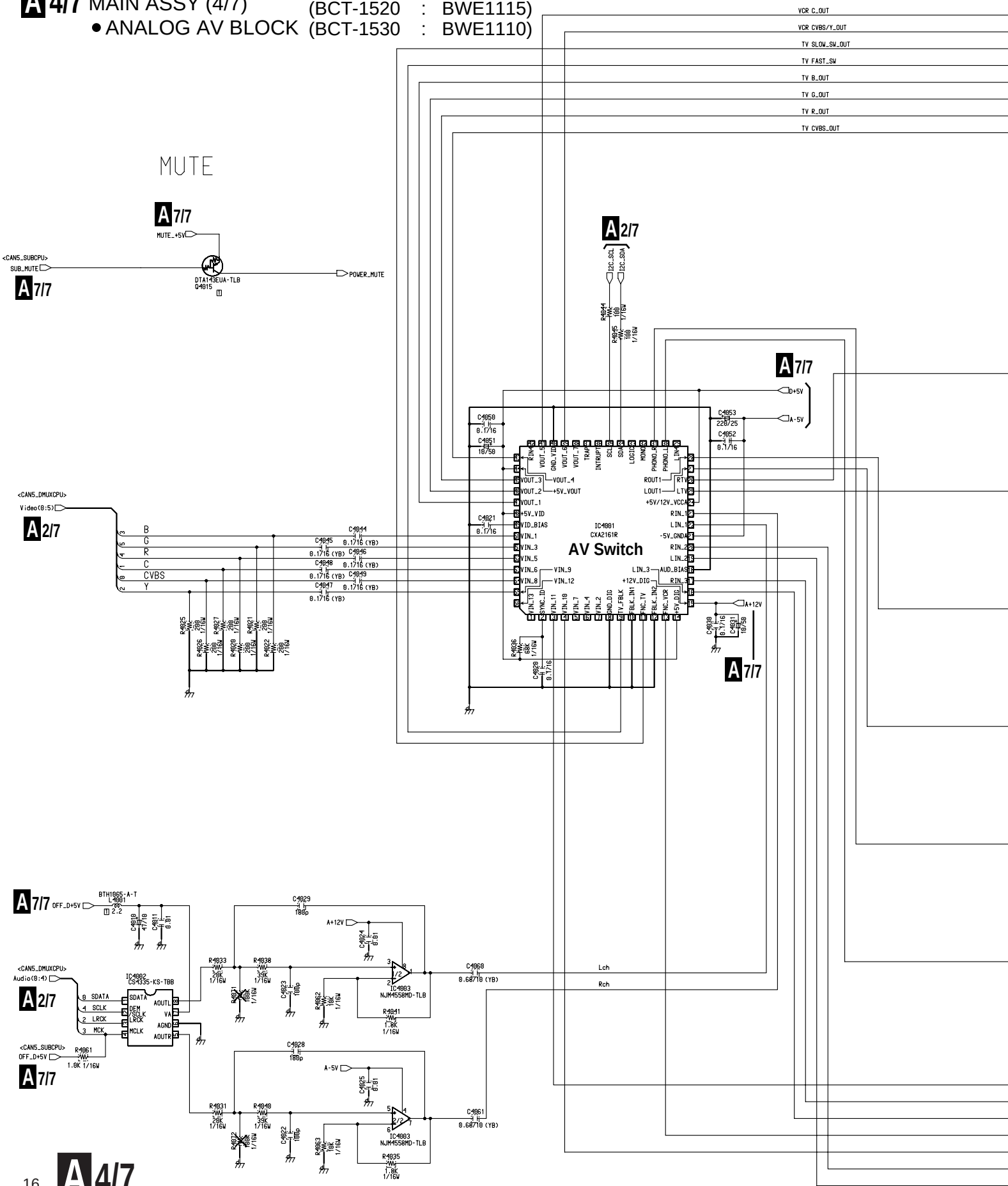
TS5, BCT-1510, BCT-1520, BCT-1530

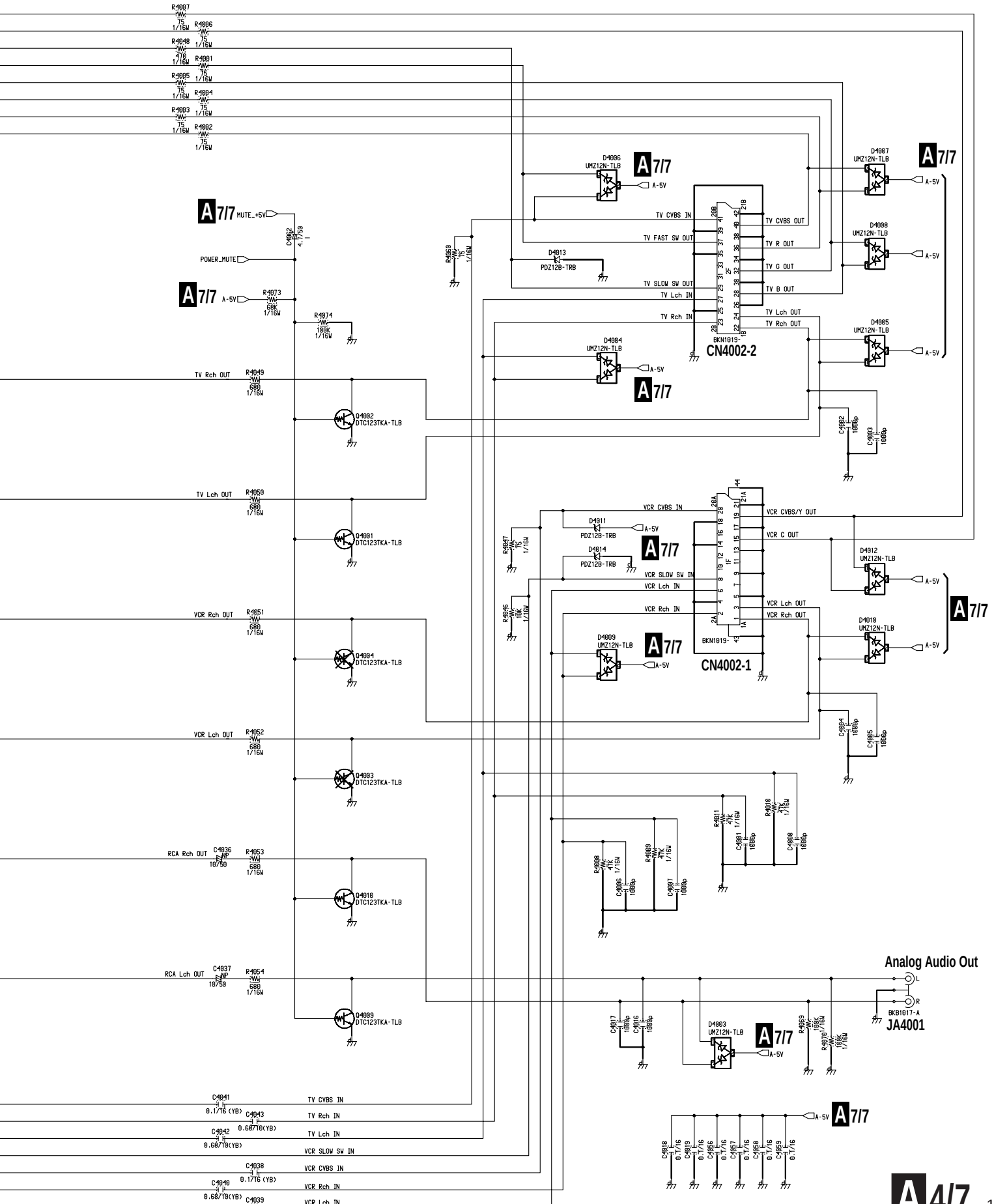
3.5 MAIN ASSY (4/7)

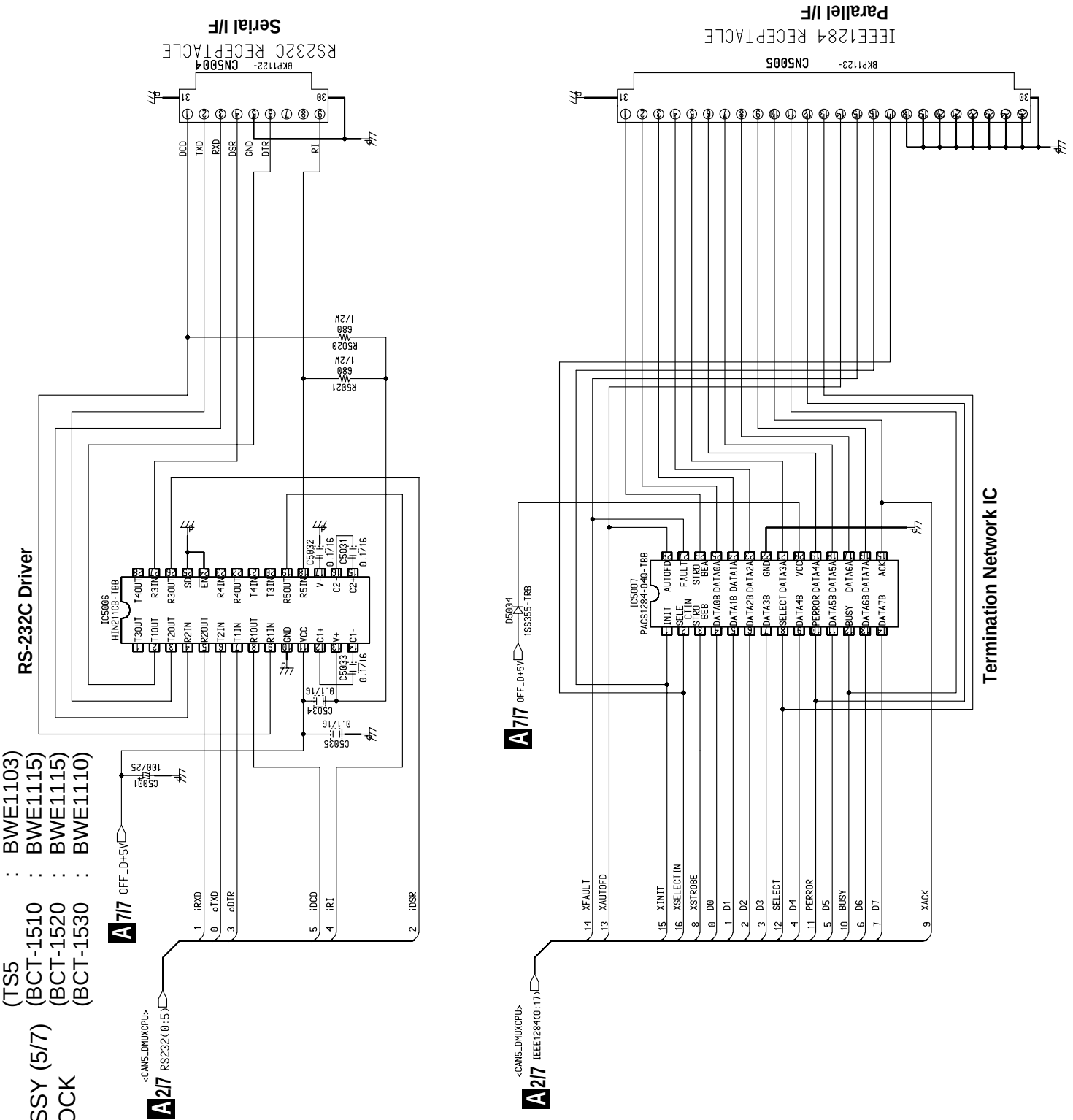
(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)

A 4/7 MAIN ASSY (4/7)

- ANALOG AV BLOCK




Analog Audio Out
JA4001
CN4002-2
CN4002-1
TV CVBS IN
TV FAST SW OUT
TV SLOW SW OUT
TV Lch IN
TV Rch IN
TV CVBS OUT
TV R OUT
TV G OUT
TV B OUT
TV Lch OUT
TV Rch OUT
VCR CVBS IN
VCR SLOW SW IN
VCR Lch IN
VCR Rch IN
VCR CVBS/Y OUT
VCR C OUT
VCR Lch OUT
VCR Rch OUT
MUTE_+5V
POWER_MUTE
A-5V
TV Rch OUT
TV Lch OUT
VCR Rch OUT
VCR Lch OUT
RCA Rch OUT
RCA Lch OUT
D4001 DTC123TKA-TLB
D4002 DTC123TKA-TLB
D4003 DTC123TKA-TLB
D4004 DTC123TKA-TLB
D4009 DTC123TKA-TLB
D4010 DTC123TKA-TLB
D4004 UMZ12N-TLB
D4005 UMZ12N-TLB
D4006 UMZ12N-TLB
D4007 UMZ12N-TLB
D4008 UMZ12N-TLB
D4009 UMZ12N-TLB
D4010 UMZ12N-TLB
D4011 UMZ12N-TLB
D4012 UMZ12N-TLB
D4013 PDZ12B-TRB
D4014 PDZ12B-TRB
BKB1017-A
BKN1019-



(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)

MAIN ASSY (5/7)
- IO BLOCK

A 5/7

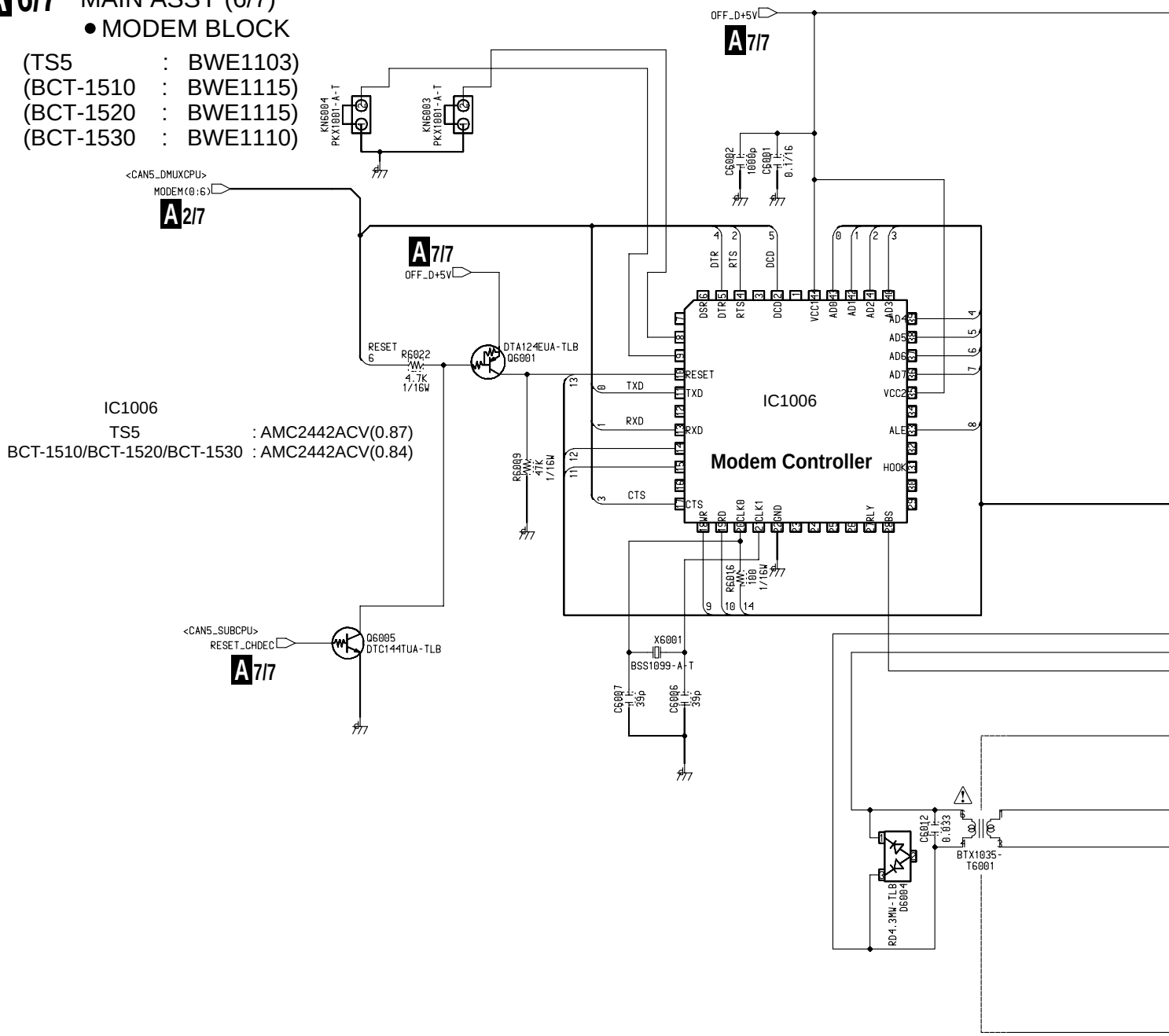
TS5, BCT-1510, BCT-1520, BCT-1530

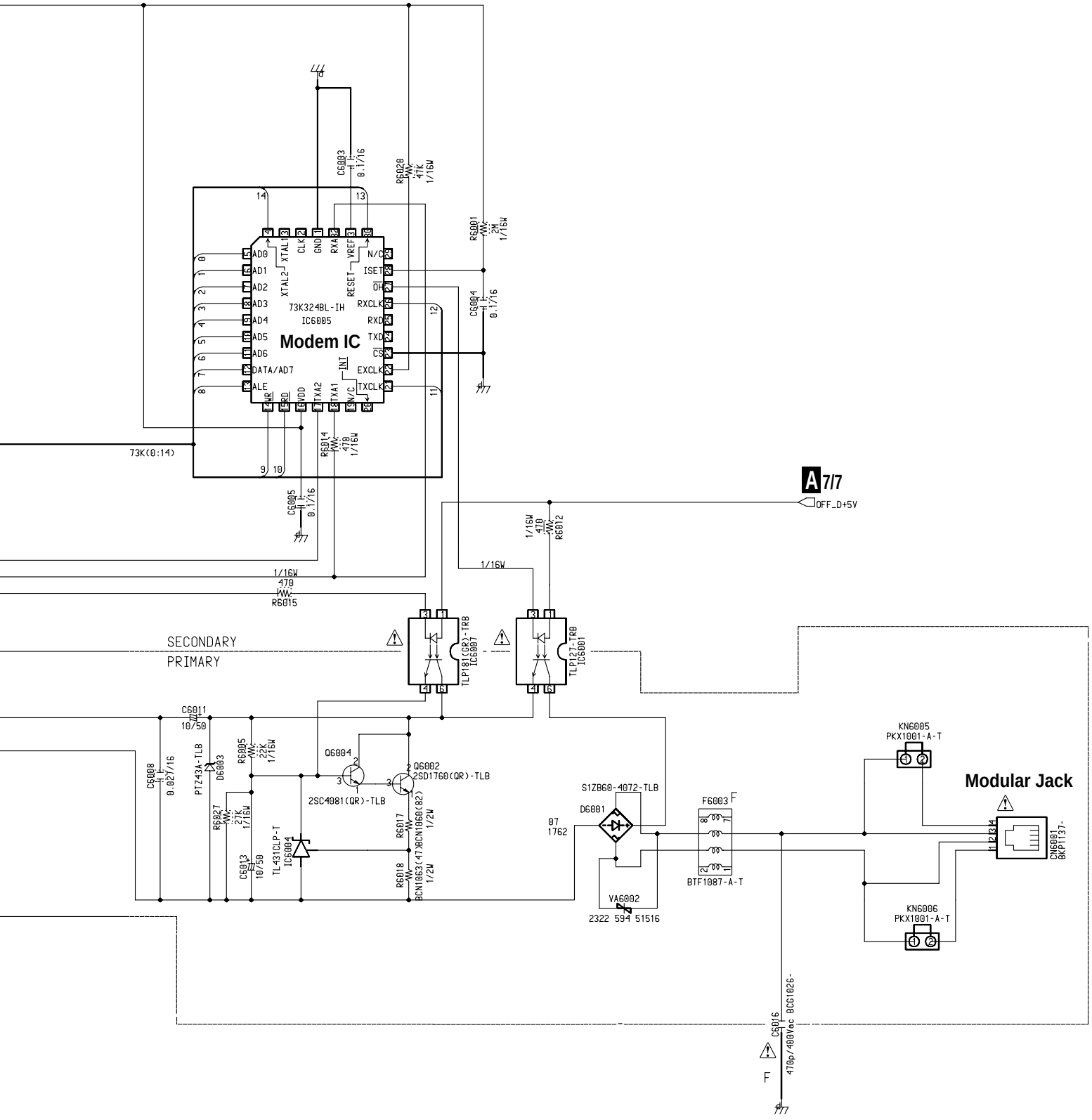
3.7 MAIN ASSY (6/7)

A 6/7 MAIN ASSY (6/7)

- MODEM BLOCK

(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)



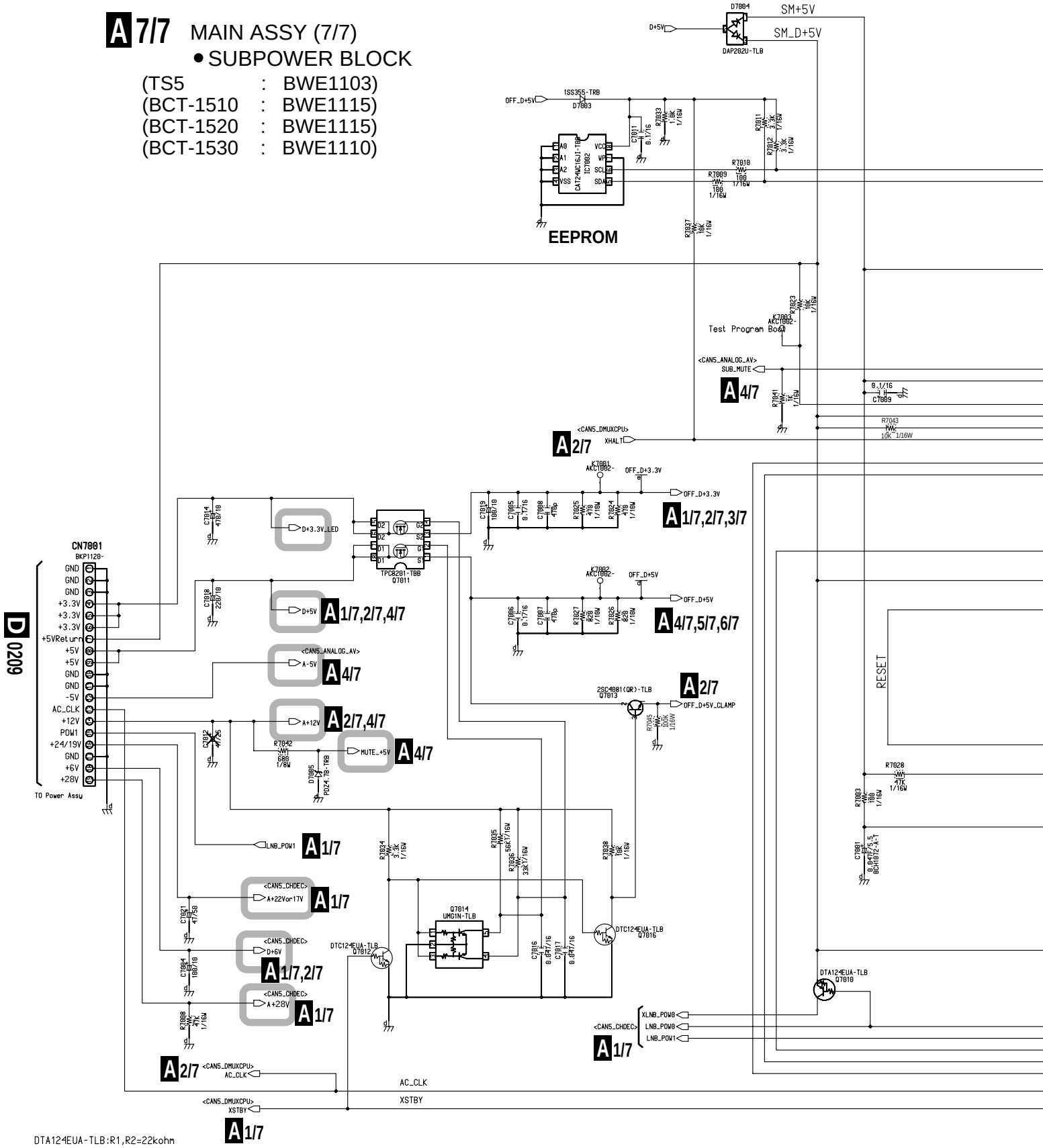

Modem IC
73K324BL-IH
IC6005
73K(0:14)
SECONDARY
PRIMARY
A7/7
OFF_D+5V
TLP181(GR)-TRB
IC6007
TLP127-TRB
IC6001
Q6004
2SC4081(QR)-TLB
Q6002
2SD1760(QR)-TLB
S1ZB60-4072-TLB
D6001
F6003
BTF1087-A-T
VA6002
2322 594 51516
KN6005
PKX1001-A-T
KN6006
PKX1001-A-T
Modular Jack
TL431CLP-T
IC6004
PTZ43A-TLB
D6003
BCN1063(47)BCN1060(82)
470p/400Vac BCG1026-

3.8 MAIN ASSY (7/7)

A 7/7 MAIN ASSY (7/7)

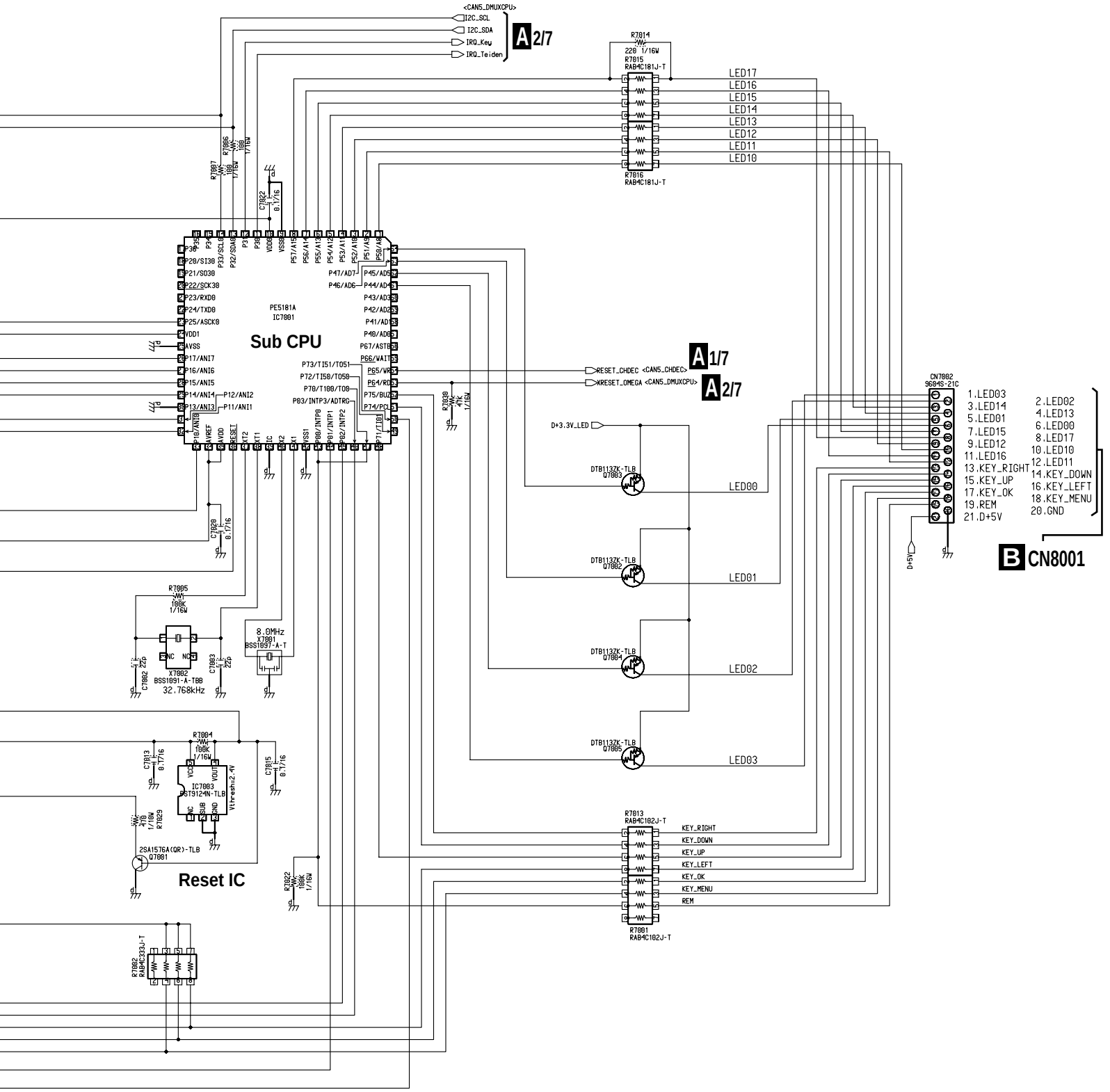
- SUBPOWER BLOCK

(TS5 : BWE1103)
(BCT-1510 : BWE1115)
(BCT-1520 : BWE1115)
(BCT-1530 : BWE1110)

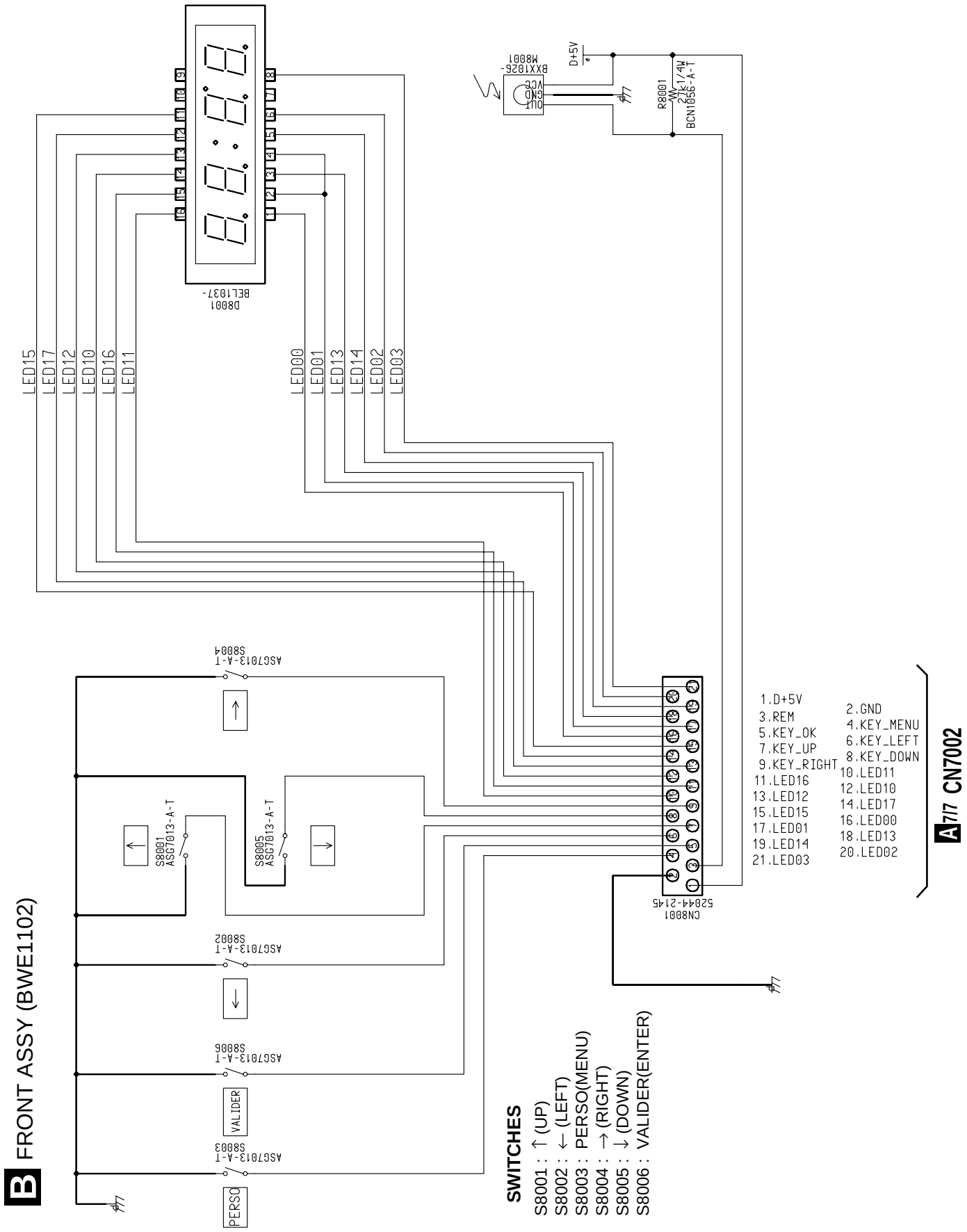


DTA124EUA-TLB:R1,R2=22kohm
DTC124EUA-TLB:R1,R2=22kohm
DTB113ZK-TLB:R1=1kohm,R2=10kohm
BTH1065-A-T:L=2.2uH

: The power supply is shown with the marked box.

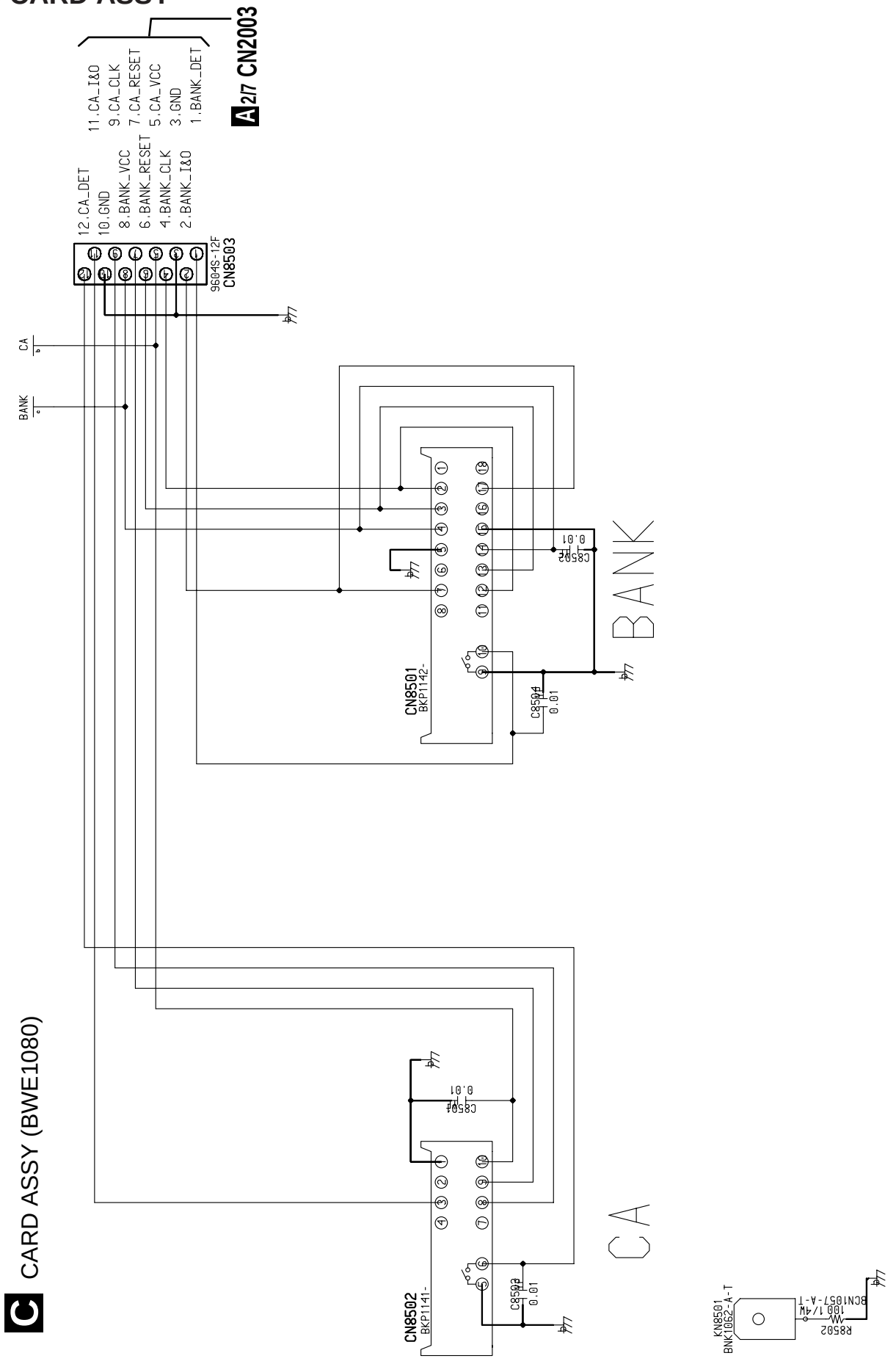


3.9 FRONT ASSY



B FRONT ASSY (BWE1102)

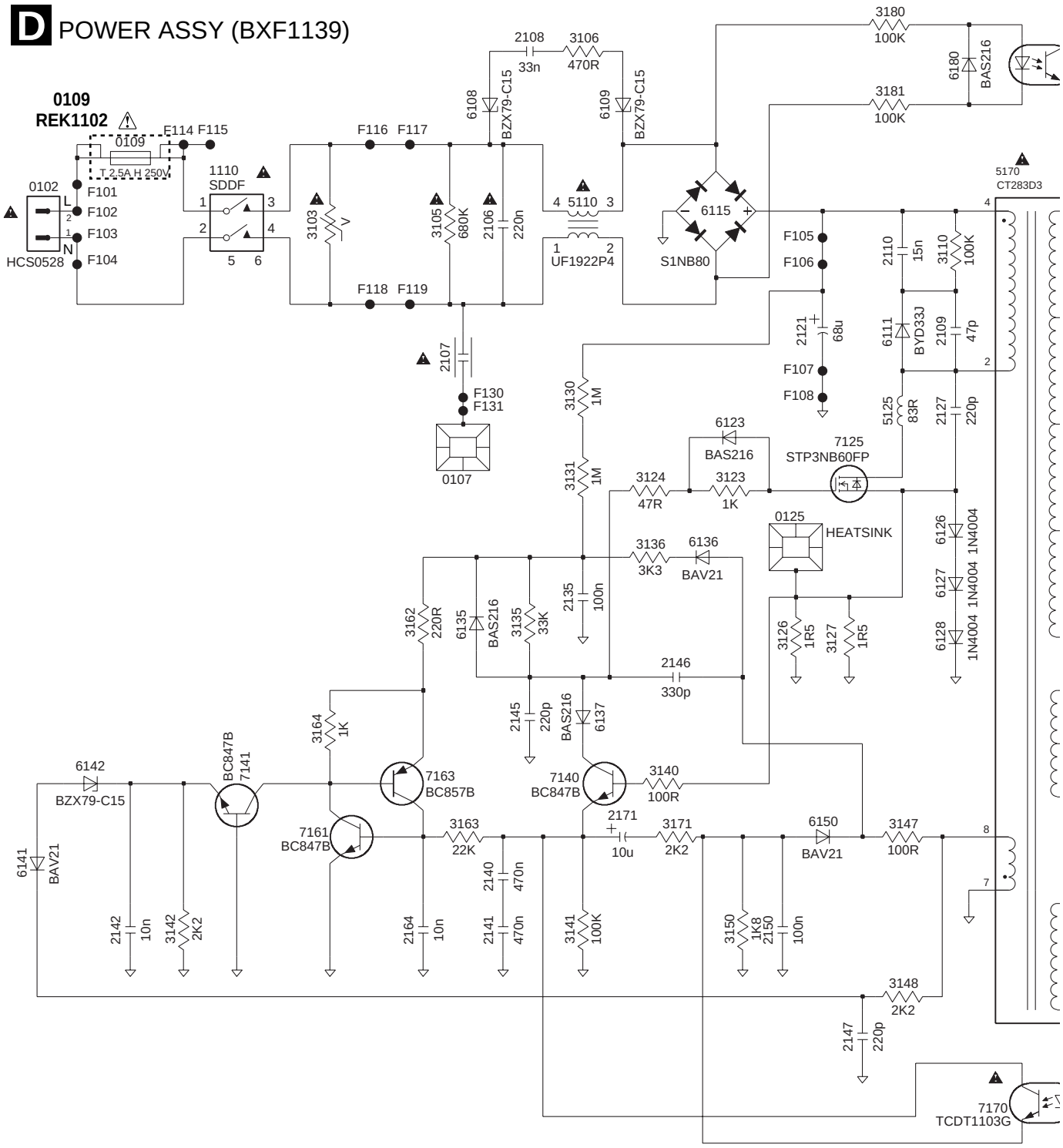
3.10 CARD ASSY



TS5, BCT-1510, BCT-1520, BCT-1530

3.11 POWER ASSY

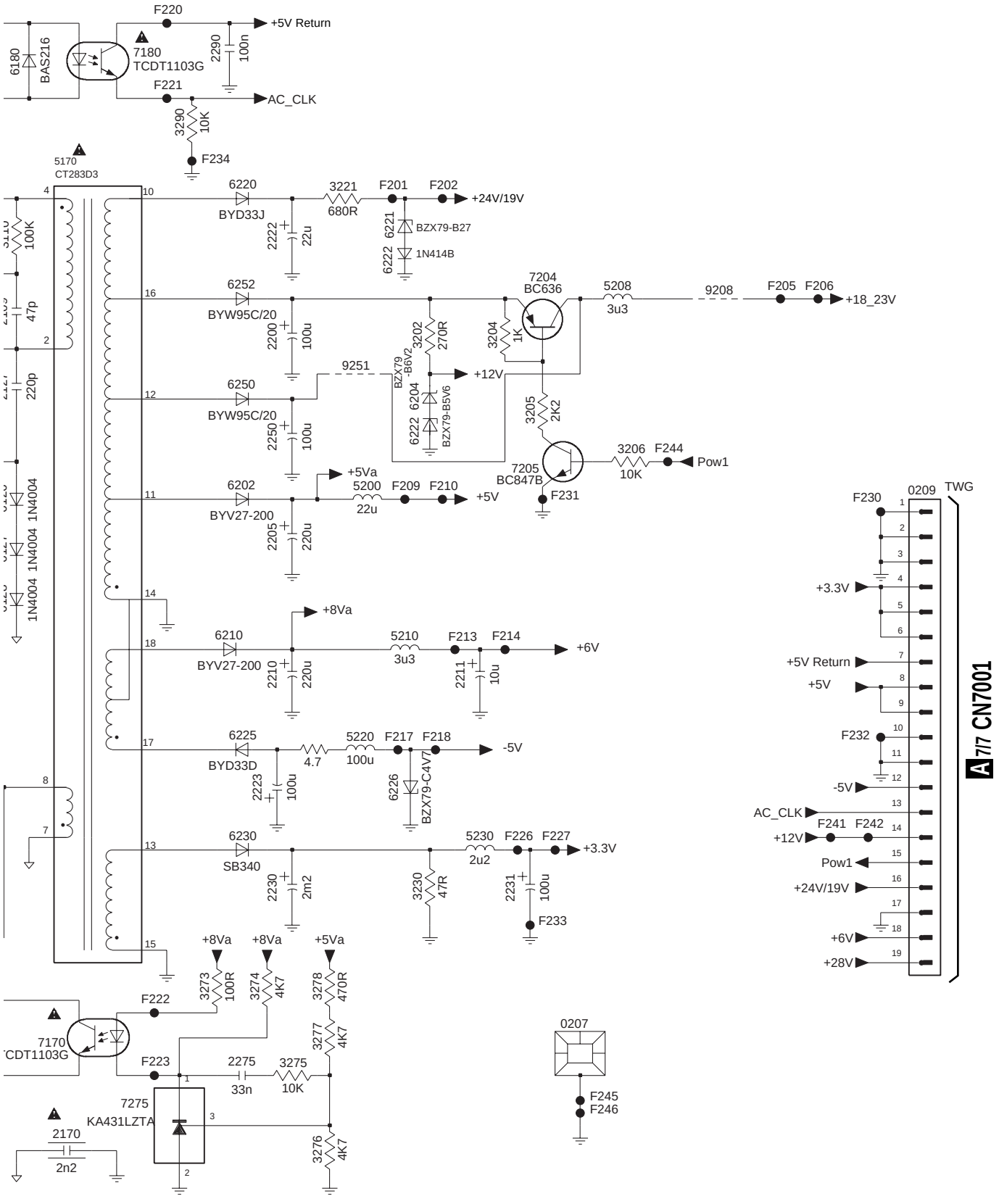
D POWER ASSY (BXF1139)



Fuse 0109 (REK1102) : Only this part is supplied as a service part..

● NOTE FOR FUSE REPLACEMENT

CAUTION – FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.


F220
+5V Return
6180
BAS216
7180
TCDT1103G
2290
100n
F221
AC_CLK
3290
10K
F234
5170
CT283D3
6220
BYD33J
3221
680R
F201
F202
+24V/19V
2222
22u
6221
BZX79-B27
6222
1N414B
7204
BC636
5208
3u3
9208
F205
F206
+18_23V
6252
BYW95C/20
2200
100u
3202
270R
3204
1K
9251
BZX79-B6V2
+12V
6204
BZX79-B5V6
6250
BYW95C/20
2250
100u
3205
2K2
3206
F244
Pow1
10K
7205
BC847B
F231
+5Va
5200
22u
F209
F210
+5V
6202
BYV27-200
2205
220u
+8Va
6210
BYV27-200
5210
3u3
F213
F214
+6V
2210
220u
2211
10u
6225
BYD33D
4.7
5220
100u
F217
F218
-5V
2223
100u
6226
BZX79-C4V7
6230
SB340
5230
2u2
F226
F227
+3.3V
2230
2m2
3230
47R
2231
100u
F233
+8Va
+8Va
+5Va
3273
100R
3274
4K7
3278
470R
3277
4K7
F222
7170
CDT1103G
F223
2275
33n
3275
10K
7275
KA431LZTA
2170
2n2
3276
4K7
0207
F245
F246
0209
TWG
F230
+3.3V
+5V Return
+5V
F232
-5V
AC_CLK
F241
F242
+12V
Pow1
+24V/19V
+6V
+28V
A7/7 CN7001
100K
47p
220p
1N4004
1N4004
1N4004
1N4004

4. PCB CONNECTION DIAGRAM

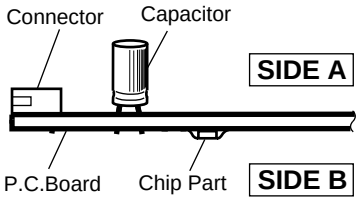
4.1 FRONT ASSY

NOTE FOR PCB DIAGRAMS :

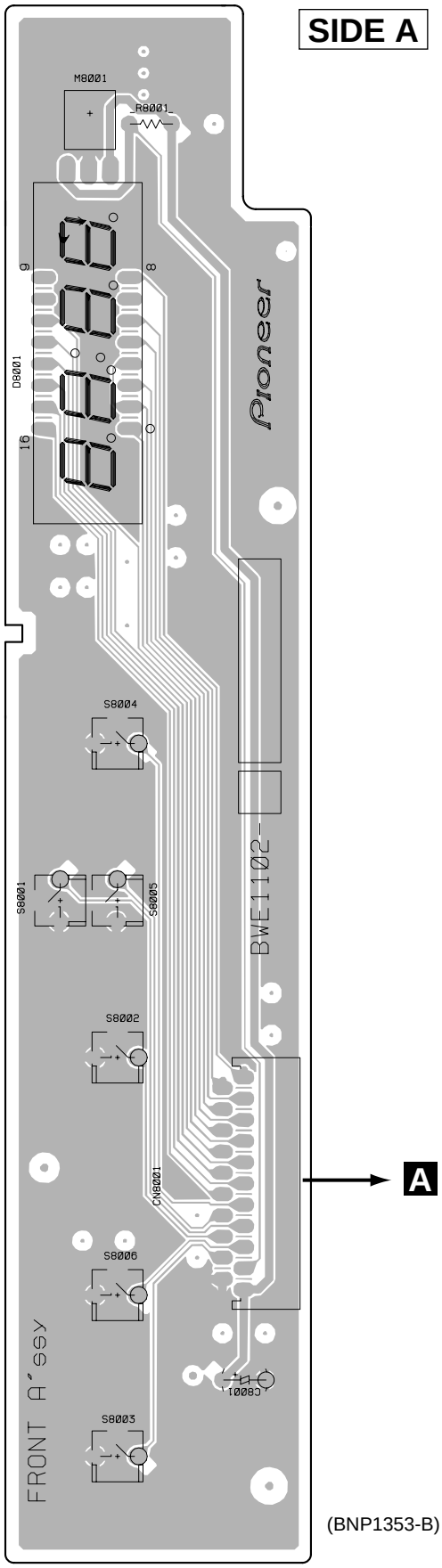
1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator

3. The parts mounted on this PCB include all necessary parts for several destinations.
   For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams.



B FRONT ASSY



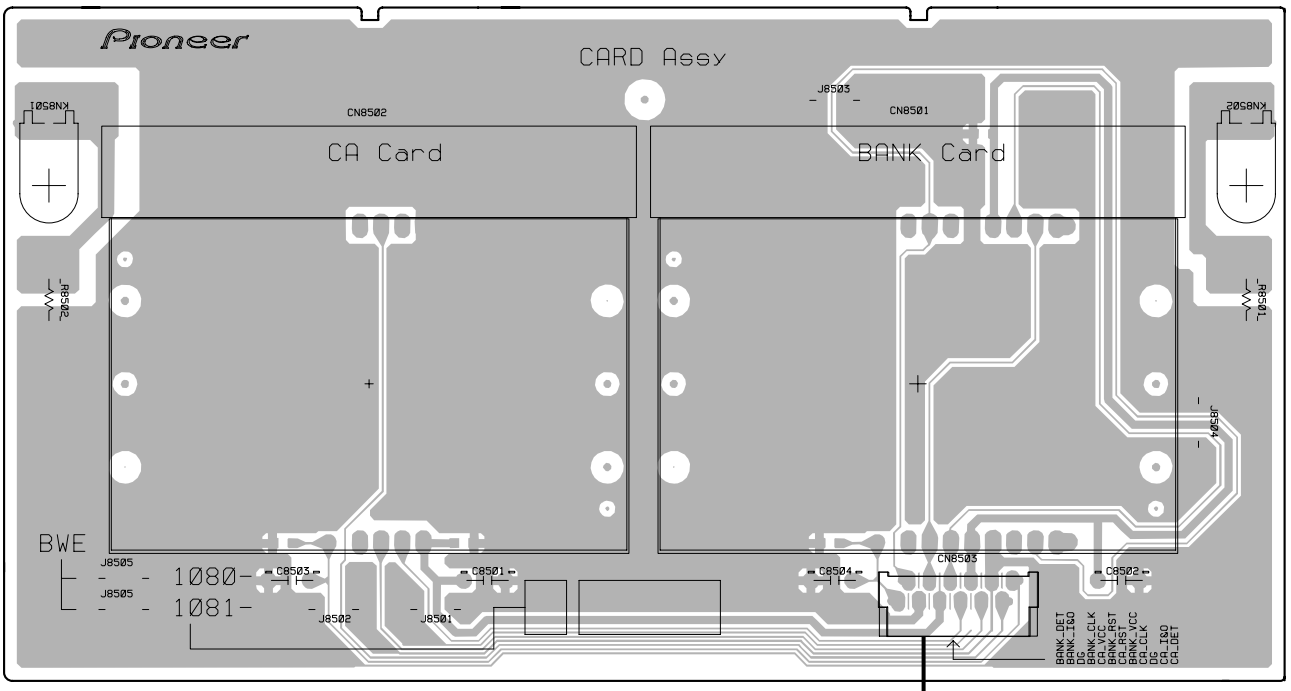
A CN7002

(BNP1353-B)

4.2 CARD ASSY

C CARD ASSY

SIDE A



(BNP1335-C)

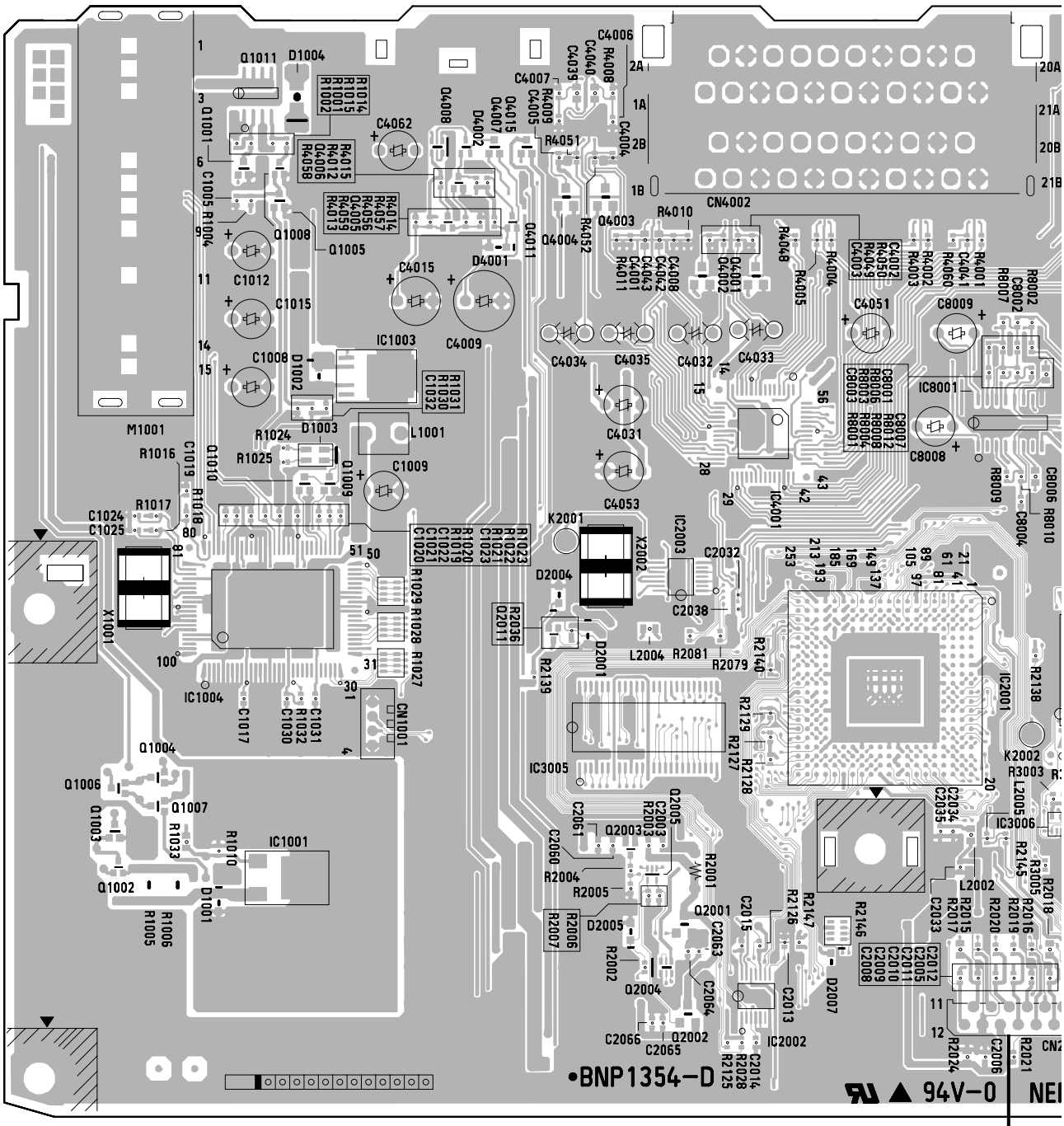
A CN2003

4.3 MAIN ASSY

A MAIN ASSY

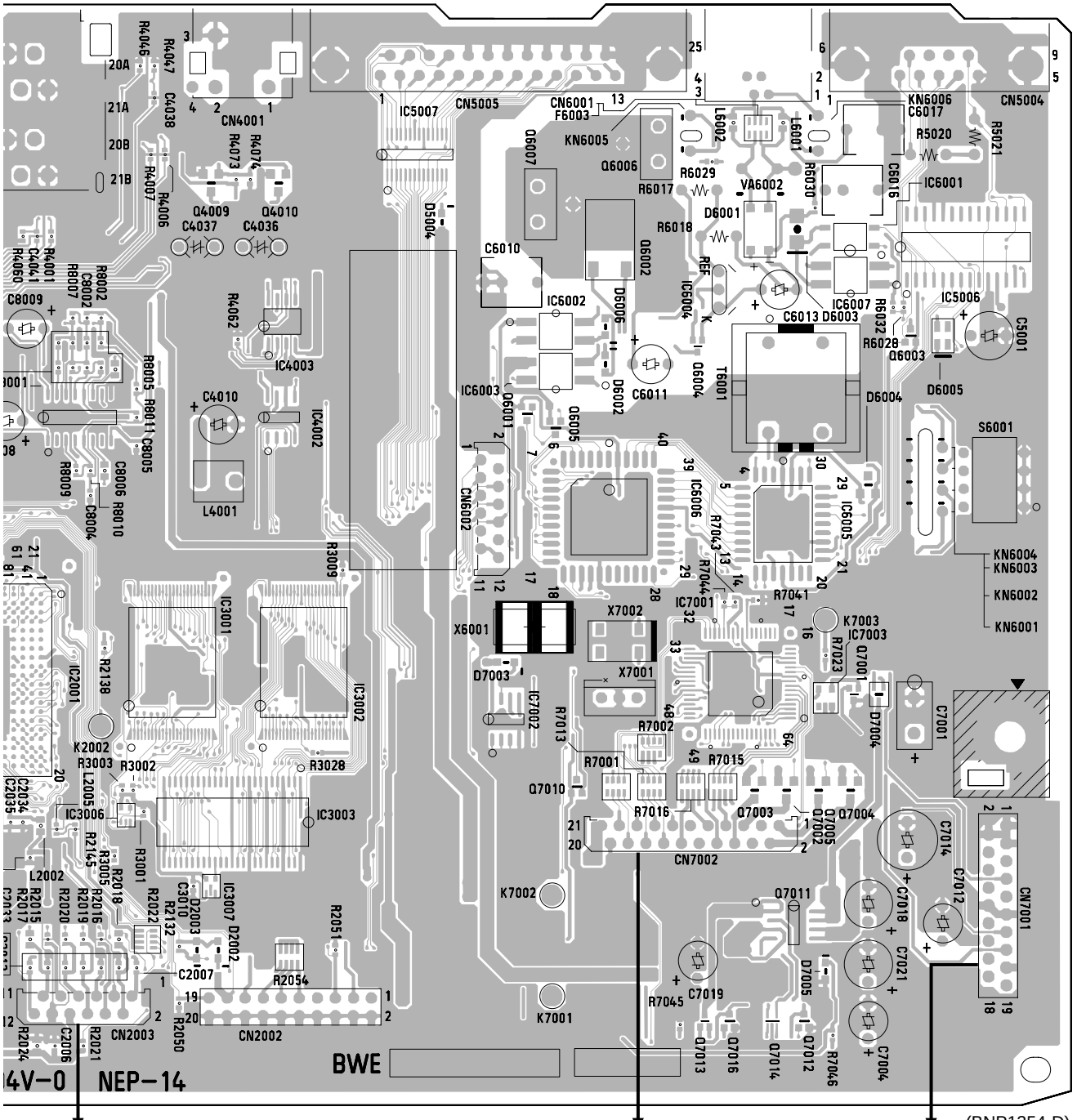
TUNER
MODULE

VCR SCART
TV SCART



Q1001 Q1011 Q4008 Q4007 Q4015
Q1008 Q4011 Q4004 Q4003 Q4002 Q4001
IC1003 IC4001 IC8001
IC1004 Q1009 Q2011 IC2003 IC2001
Q1006 Q1003 Q1004 Q1007 IC3005 Q2003 Q2005 IC3
Q1002 IC1001 Q2004 Q2002 Q2011 IC2002

SIDE A

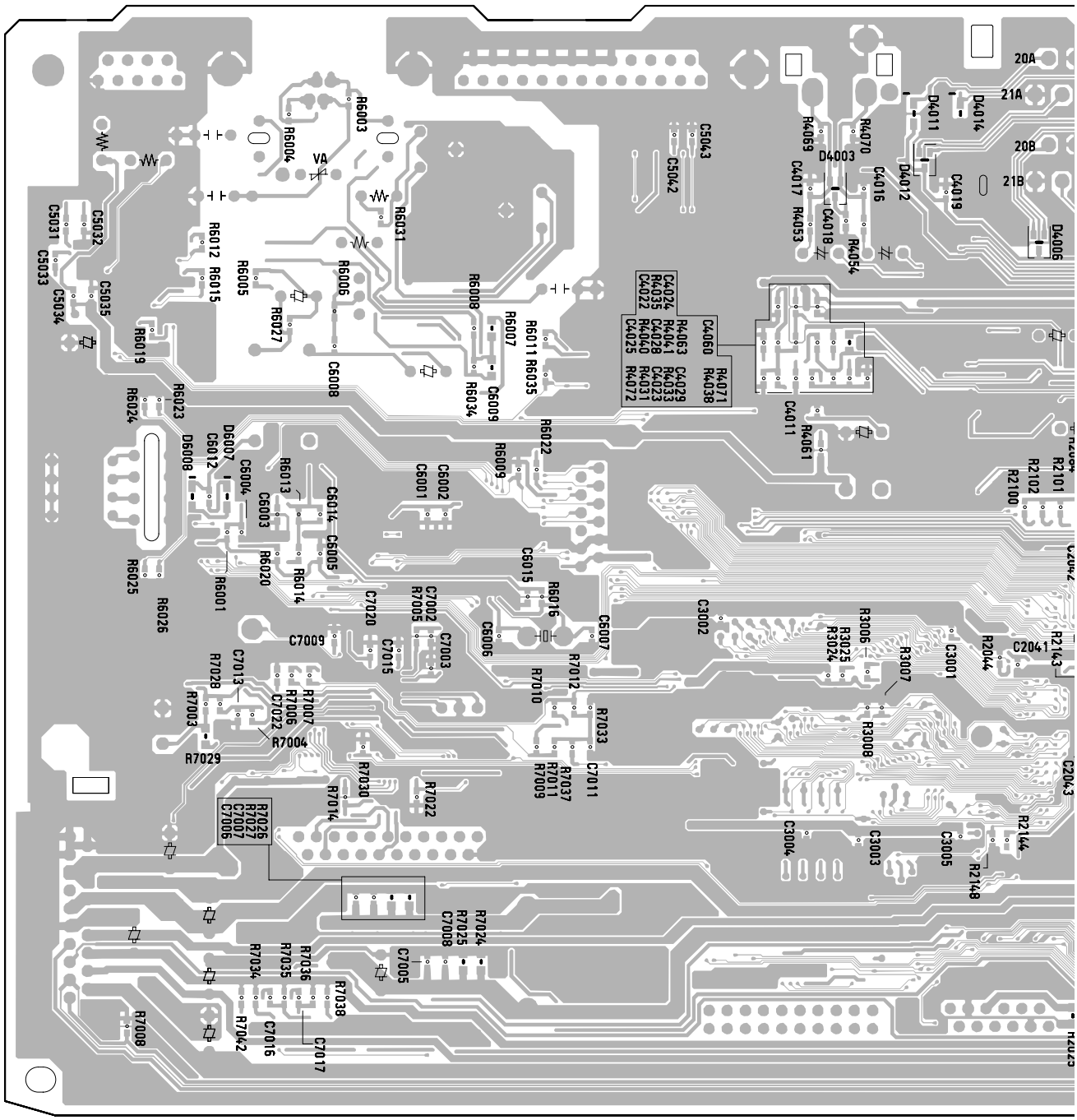


(BNP1354-D)

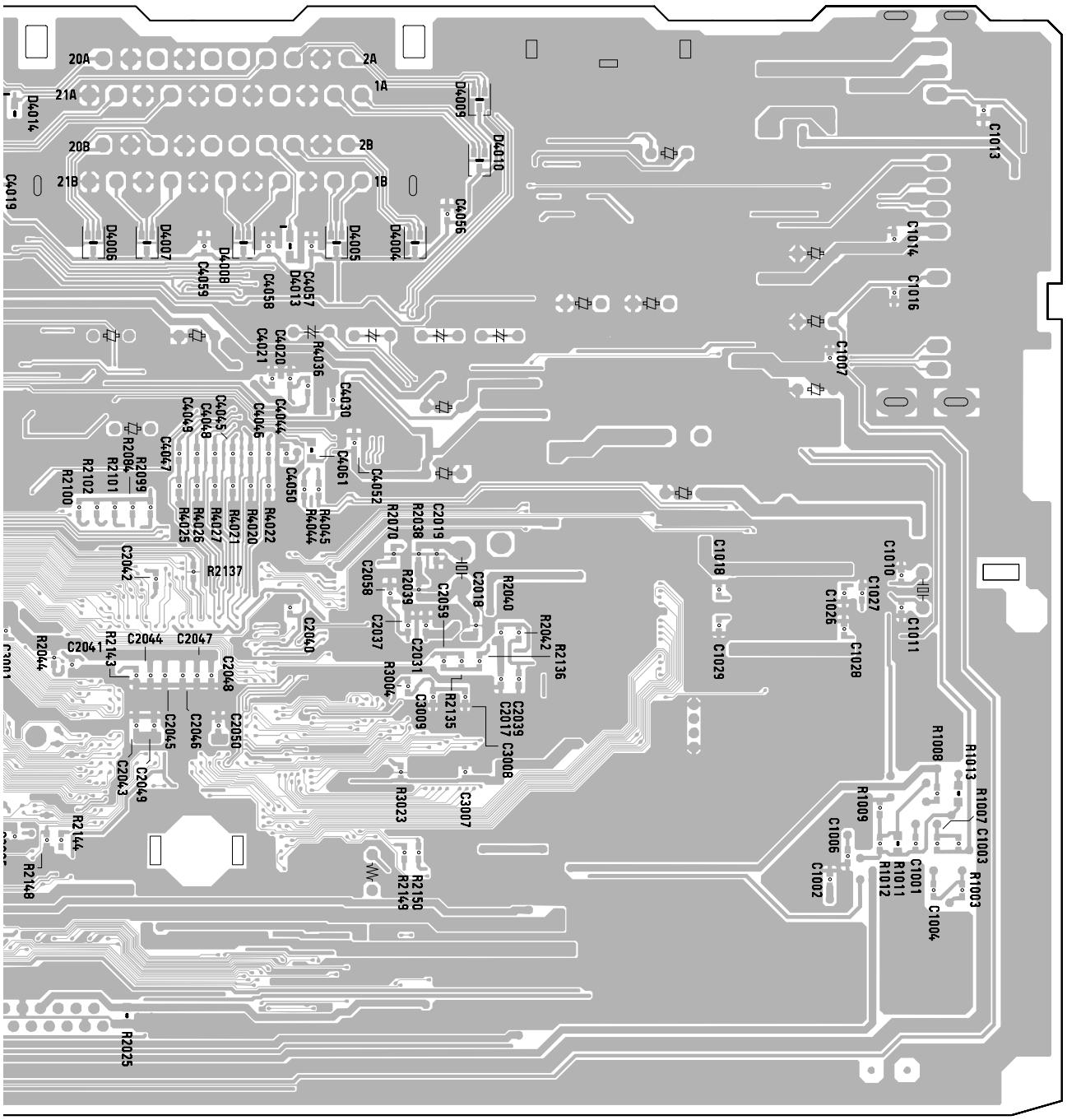
C CN8503 B CN8001 D 0209

IC5007 Q6007 Q6006
Q4009 Q4010 IC6002 IC6003 Q6002 IC6004 IC6001 IC6007 IC5006
IC8001 IC4003 IC4002 Q6001 Q6005 IC6006 IC6005 Q6003
IC3001 IC3002 IC7002 Q7010 IC7001 IC7003 Q7001
IC3006 IC3003 Q7003 Q7002 Q7005 Q7004
IC3007 Q7013 Q7016 Q7014 Q7011 Q7012

A MAIN ASSY


20A
21A
20B
21B
D4011
D4014
D4012
D4003
D4006
R4069
R4070
C4017
C4016
C4019
R4053
C4018
R4054
C5043
C5042
C4060
R4071
R4038
C4011
R4061
R2101
R2102
R2100
R6003
R6004
VA
R6031
C5031
C5032
C5033
C5034
C5035
R6012
R6015
R6005
R6027
R6006
R6008
R6007
R6011
R6035
R6034
C6009
C6008
R6019
R6023
R6024
D6007
D6008
C6012
C6004
C6003
R6013
C6014
C6005
R6020
R6014
R6001
R6025
R6026
R6022
R6009
C6002
C6001
C6015
R6016
C6006
C6007
C3002
C7020
C7002
R7005
C7003
C7009
C7015
R7028
C7013
R7003
R7029
R7007
R7006
C7022
R7004
R7012
R7010
R7033
C7011
R7037
R7011
R7009
R7030
R7014
R7022
R7026
R7027
C7007
C7006
R7024
R7025
C7008
C7005
R7034
R7035
R7036
R7038
R7008
R7042
C7016
C7017
R3006
R3025
R3024
C3001
R2044
C2041
R2143
R3007
R3008
C2043
C3004
C3003
C3005
R2144
R2148

SIDE B



(BNP1354-D)

TS5, BCT-1510, BCT-1520, BCT-1530

5. PCB PARTS LIST

NOTES: ●*Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
●*The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
●*When ordering resistors, first convert resistance values into code form as shown in the following examples.*
Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).
560 Ω → 56 × 10¹ → 561 ..... RD1/4PU 5 6 1 J
47k Ω → 47 × 10³ → 473 ..... RD1/4PU 4 7 3 J
0.5 Ω → R50 ..... RN2H R 5 0 K
1 Ω → 1R0 ..... RS1P 1 R 0 K
Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).
5.62k Ω → 562 × 10¹ → 5621 ..... RN1/4PC 5 6 2 1 F

■ CONTRAST OF PCB ASSEMBLIES

Mark	Symbol and Description	Part No.				Remarks
		TS5	BCT-1510	BCT-1520	BCT-1530	
		NYXK/FR NYXK/FR1 NYXK/FR2 NYXK/FR2	NYXK/SP	NYXK/IT	NYWXKPL	
	MAIN ASSY	BWE1103	BWE1115	BWE1115	BWE1110	
	FRONT ASSY	BWE1102	BWE1102	BWE1102	BWE1102	
	CARD ASSY	BWE1080	BWE1080	BWE1080	BWE1080	
⚠	POWER ASSY	BXF1139	BXF1139	BXF1139	BXF1139	

A MAIN ASSY

BWE1103, BWE1115 and BWE1110 are constructed the same except for the following:

Mark	Symbol and Description	Part No.			Remarks
		BWE1103	BWE1115	BWE1110	
	IC1004	TDA8083H	TDA8083H	TDA8083H/E	
	IC2001	STI5512AWE	STI5512AWE	STI5512AWE/E	
	IC6006	AMC2442ACV(0.87)	AMC2442ACV(0.84)	AMC2442ACV(0.84)	

●MAIN ASSY IC3002 CONTRAST TABLE

IC3002 (16M FLASH Memory) is different according to the model types as the following tabel.

Mark	Symbol and Description	Part No.							Remarks
		TS5 /NYXK/FR	TS5 /NYXK/FR1	TS5 /NYXK/FR2	TS5 /NYXK/FR3	BCT-1510 /NYXK/SP	BCT-1520 /NYXK/IT	BCT-1530 /NYWXKPL	
	IC3002 (16M FLASH Memory)	BGC1059-A-AV	BGC1060-A-AV	BGC1061-A-AV	BGC1062-A-AV	BGC1063-A-AV	BGC1064-A-AV	BGC1065-A-AV	

Mark	No.	Description	Part No.
A		**MAIN ASSY**	
		SEMICONDUCTORS	
	IC6005		73K324BL-IH
	IC2003		74LVU04PW
	IC6006		AMC2442ACVF(0.87)
	IC1003		BA05SFP
	IC7002		CAT24WC16JI
	IC4002		CS4335-KS
	IC4001		CXA2161R
	IC5006		HIN211CB
	IC3005		HYB39S16160AT-10
	IC1001		NJM317DL1
	IC4003		NJM4558MD
	IC3003		NT56V1616A0T-8
	IC5007		PACS1284-04Q
	IC7001		PE5181A
	IC7003		PST9124N
	IC2002		SN74ACT08PWR
	IC2001		STI5512MWD
	IC3001		BGC1058-A-AV
	IC3002		See IC3002 Contrast table
	IC3006		TC7SZ126FU
	IC1004		TDA8083H
	IC6004		TL431CLP
⚠	IC6001		TLP127
⚠	IC6007		TLP181(GR)

Mark	No.	Description	Part No.
	Q1002,Q2003,Q7001		2SA1576A
	Q2001,Q2002		2SC2411K
	Q1008,Q2011,Q6004,Q7013		2SC4081
	Q6002		2SD1760
	Q6001,Q7010		DTA124EUA
	Q4015		DTA143EUA
	Q7002-Q7005		DTB113ZK
	Q4001,Q4002,Q4009,Q4010		DTC123TKA
	Q1001,Q1003-Q1007,Q7012,Q7016		DTC124EUA
	Q6005		DTC144TUA
	Q7011		TPC8201
	Q1011		TPC8301
	Q2005		UMA10N
	Q2004		UMD2N
	Q7014		UMG1N
	D1002,D5004,D7003		1SS355
	D7004		DAP202U
	D2001		HVU356
	D4011,D4013,D4014		PDZ12B
	D2007,D7005		PDZ4.7B
	D2005		PDZ5.6B
	D2004		PDZ8.2B
	D6003		PTZ43A
	D1004		RB160L-40
	D1001,D2002,D2003		RB501V-40
	D6004		RD4.3MW
	D6001		S1ZB60-4072
	D4003-D4010,D4012		UMZ12N
⚠	VA6002		2322 594 51516

COILS AND FILTERS

Mark	No.	Description	Part No.
⚠	F6003		BTF1087
	L1001,L4001		BTH1065
⚠	T6001		BTX1035
	L2005		BTX1036
	L2002,L2004		DTL1038

CAPACITORS

Mark	No.	Description	Part No.
⚠	C6016 (470pF/AC250V)		BCG1026
	C7001 (0.047F/5.5V)		BCH1072
	C4022,C4023		CCSRCH101J50
	C4028,C4029		CCSRCH181J50
	C7002,C7003		CCSRCH220J50
	C2005-C2008,C2013,C2014,C2018		CCSRCH221J50
	C1010,C1011,C2010,C2011,C2019		CCSRCH330J50
	C6006,C6007		CCSRCH390J50
	C1009,C4031,C6011,C6013		CEAK100M50
	C7004,C7019		CEAK101M10
	C5001		CEAK101M25
	C7018		CEAK221M10
	C4053		CEAK221M25
	C1008,C1012		CEAK470M16
	C7014		CEAK471M10
	C4036,C4037		CEANP100M50
	C4051		CEAT100M50
	C4010		CEAT470M16
	C7021		CEAT470M50
	C4062		CEAT4R7M50
	C4039,C4040,C4042,C4043		CKSQYB684K10
	C4060,C4061		CKSQYB684K10
	C2034,C2058,C4001-C4008		CKSRYB102K50
	C4016,C4017,C6002		CKSRYB102K50
	C1002,C1006,C1007,C1013,C1014		CKSRYB103K50
	C1016,C2031,C2033,C2035,C2037		CKSRYB103K50
	C2060,C4011,C4024,C4025		CKSRYB103K50
	C1019,C1024-C1026,C4038,C4041		CKSRYB104K16
	C4044-C4049		CKSRYB104K16
	C1032		CKSRYB153K50
	C6008		CKSRYB273K16
	C1001		CKSRYB332K50
	C6012		CKSRYB333K25
	C2059,C2061,C7007,C7008		CKSRYB471K50
	C7016,C7017		CKSRYB473K16
	C1017,C1018,C1020-C1023		CKSRYF104Z16
	C1027-C1031,C2003,C2015,C2032		CKSRYF104Z16
	C2038-C2050,C3001-C3005		CKSRYF104Z16
	C3007-C3009,C4018-C4021,C4030		CKSRYF104Z16
	C4050,C4052,C4056-C4059		CKSRYF104Z16
	C5031-C5035,C6001,C6003-C6005		CKSRYF104Z16
	C7005,C7006,C7009,C7011,C7013		CKSRYF104Z16
	C7015,C7020,C7022		CKSRYF104Z16
	C2063,C2065		CKSRYF224Z16
	C1004,C1005,C2017		CKSRYF474Z16

RESISTORS

Mark	No.	Description	Part No.
	R5020,R5021 (680Ω/1/2W)		BCN1046
	R6017 (82Ω/1/2W)		BCN1060
	R6018 (47Ω/1/2W)		BCN1063
	R2146,R7001,R7013		RAB4C102J
	R2022,R2054		RAB4C103J
	R7015,R7016		RAB4C181J
	R7002		RAB4C333J
	R2001		RD1/2VM3R3J
	R2017		RS1/10S331J
	R1011,R1013,R1033		RS1/10S3601F
	R2024,R2025,R7024,R7025,R7029		RS1/10S471J
	R7042		RS1/10S681J
	R2018		RS1/10S750J
	R7026,R7027		RS1/10S821J
	R1010		RS1/16S1200F
	R1012		RS1/16S1202F
	R4020-R4022,R4025,R4026		RS1/16S2000F
	R2079,R2081		RS1/16S9101F
	R1005,R1006		RS1/2S1R8J
	Other Resistors		RS1/16S□□□J

OTHERS

Mark	No.	Description	Part No.
⚠	M1001	DBS Front End	BXF1135
	CN2003	12P FFC Connector	9604S-12C
	CN7002	21P FFC Connector	9604S-21C
	JA4001	2P Pin Jack	BKB1017
	CN4002	SCART Connector	BKN1019
	CN7001	19P Plug	BKP1120
	CN5004	DSUB 9P Connector	BKP1122
	CN5005	DSUB 25P Connector	BKP1123
⚠	CN6001	4P Modular Jack	BKP1137
		Ground Plate	BNK1081
	X1001 (4MHz)		BSS1056
	X2002 (27MHz)		BSS1061
	X7002 (32.768kHz)		BSS1091
	X7001 (8.0MHz)		BSS1097
	X6001 (11.0592MHz)		BSS1099
	KN6003-KN6006	Jumper Terminal	PKX1001

Mark	No.	Description	Part No.

B FRONT ASSY

SEMICONDUCTORS

	D8001	BEL1037

SWITCHES AND RELAYS

	S8001-S8006	ASG7013

RESISTORS

	R8001 (27kΩ/1/4W)	BCN1056

OTHERS

	M8001 Remote Sensor Unit	BXX1026
	CN8001 21P FFC Connector	9607S-21F

C CARD ASSY

CAPACITORS

	C8501-C8504	CKCYF103Z50

RESISTORS

	R8502 (100Ω/1/4W)	BCN1057

OTHERS

	CN8503 12P Connector	9604S-12F
	CN8502 8Pin CARD Connector	BKP1141
	CN8501 16Pin CARD Connector	BKP1142

D

POWER ASSY

This ASSY has no service part as a assy part.
Only the fuse(0109:REK1102) is the service part as a set part. Refer to page 7.

6. ADJUSTMENT

There is no information to be shown in this chapter.

7. GENERAL INFORMATION

7.1 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

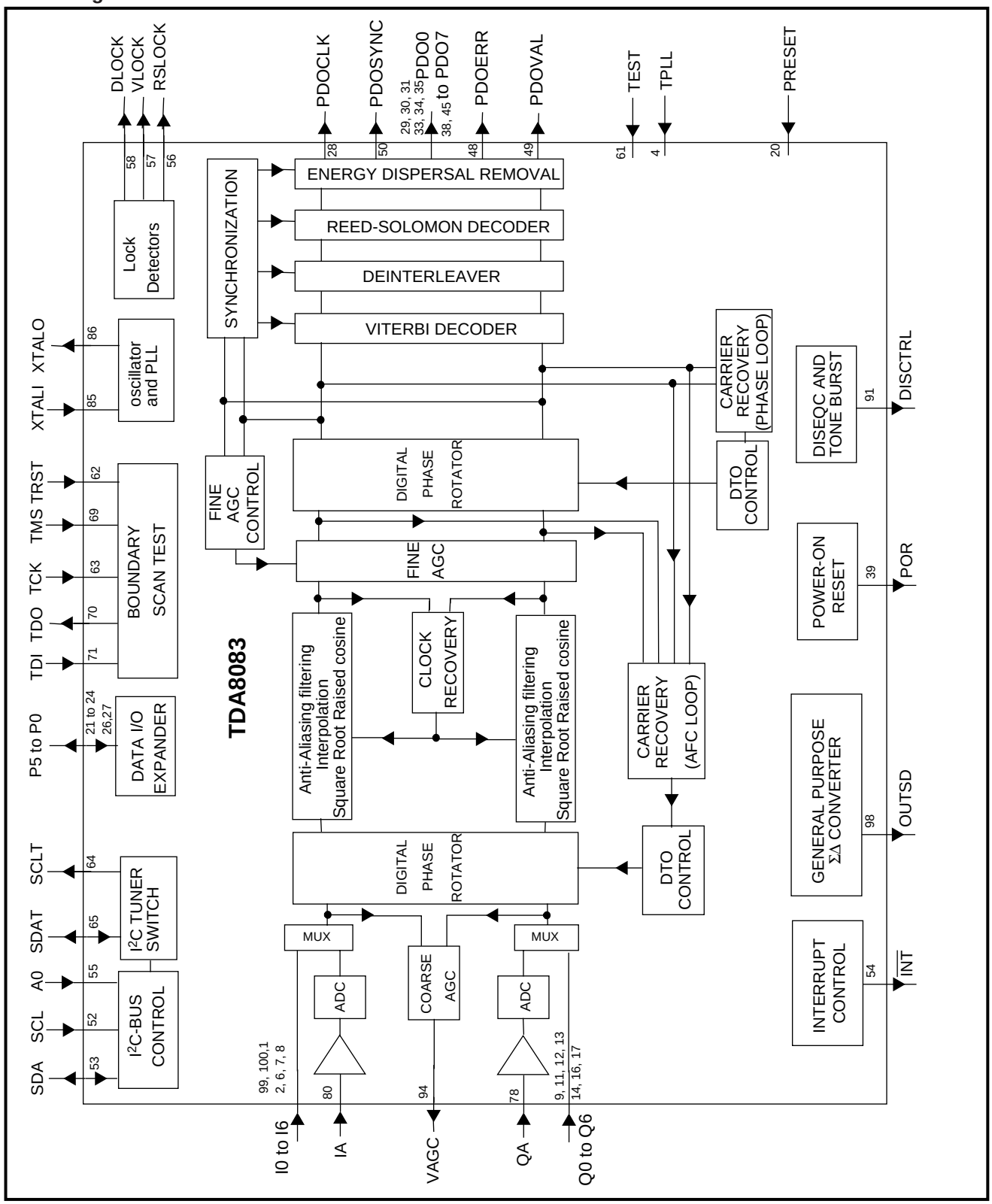
● List of IC

TDA8083H STI5512MWD CXA2161R CS4335-KS 73K324BL-IH
AMC2442ACVF(0.87) PE5181A

■ TDA8083H (MAIN ASSY(1/7) : IC1004)

• Demodulator and Decoder

●Block Diagram



●Pin Function (1/3)

PIN	SYMBOL	I/O	DESCRIPTION
1	I2	I	digital I-input bit 2 (ADC bypass)
2	I3	I	digital I-input bit 3 (ADC bypass)
3	V_{SSD1}	–	digital ground 1 (core and input periphery)
4	TPLL	I	test pin (normally connected to ground)
5	V_{SSD2}	–	digital ground 2 (core and input periphery)
6	I4	I	digital I-input bit 4 (ADC bypass)
7	I5	I	digital I-input bit 5 (ADC bypass)
8	I6	I	digital I-input bit 6 (ADC bypass - MSB)
9	Q0	I	digital Q-input bit 0 (ADC bypass - LSB)
10	V_{DDD1}	–	digital supply voltage1 (core and input periphery)
11	Q1	I	digital Q-input bit 1 (ADC bypass)
12	Q2	I	digital Q-input bit 2 (ADC bypass)
13	Q3	I	digital Q-input bit 3 (ADC bypass)
14	Q4	I	digital Q-input bit 4 (ADC bypass)
15	V_{SSD3}	–	digital ground 3 (core and input periphery)
16	Q5	I	digital Q-input bit 5 (ADC bypass)
17	Q6	I	digital Q-input bit 6 (ADC bypass - MSB)
18	V_{SSD4}	–	digital ground 4 (output periphery)
19	V_{DDD2}	–	digital supply voltage 2 (core and input periphery)
20	PRESET	I	set device into default mode
21	P3	I/O	quasi-bidirectional I/O port (bit 3)
22	P2	I/O	quasi-bidirectional I/O port (bit 2)
23	P1	I/O	quasi-bidirectional I/O port (bit 1)
24	P0	I/O	quasi-bidirectional I/O port (bit 0)
25	V_{DDD3}	–	digital supply voltage 3 (output periphery)
26	P5	I/O	quasi-bidirectional I/O port (bit 5)
27	P4	I/O	quasi-bidirectional I/O port (bit 4)
28	PDOCLK	O	output clock for transport stream bytes
29	PDO0	O	parallel data output (bit 0) - Serial data output
30	PDO1	O	parallel data output (bit 1)
31	PDO2	O	parallel data output (bit 2)
32	V_{SSD5}	–	digital ground 5 (output periphery)
33	PDO3	O	parallel data output (bit 3)
34	PDO4	O	parallel data output (bit 4)
35	PDO5	O	parallel data output (bit 5)
36	V_{SSD6}	–	digital ground 6 (core and input periphery)
37	V_{SSD7}	–	digital ground 7 (core and input periphery)
38	PDO6	O	parallel data output (bit 6)

●Pin Function (2/3)

PIN	SYMBOL	I/O	DESCRIPTION
39	POR	O	Power-on Reset
40	V_{DDD4}	–	digital supply voltage 4 (output periphery)
41	V_{DDD5}	–	digital supply voltage 5 (core and input periphery)
42	V_{SSD8}	–	digital ground 8 (core and input periphery)
43	V_{DDD6}	–	digital supply voltage 6 (core and input periphery)
44	V_{DDD7}	–	digital supply voltage 7 (output periphery)
45	PDO7	O	parallel data output (bit 7)
46	n.c.	–	not connected
47	V_{SSD9}	–	digital ground 9 (core and input periphery)
48	PDOERR	O	transport error indicator
49	PDOVAL	O	data valid indicator
50	PDOSYNC	O	transport packet synchronization signal
51	V_{SSD10}	–	digital ground 10 (output periphery)
52	SCL	I	serial clock of I^2C-bus
53	SDA	I/O	serial data of I^2C-bus
54	$\overline{INT}$	O	interrupt output (active LOW)
55	A0	I	I^2C hardware address
56	RSLOCK	O	Reed-Solomon lock indicator
57	VLOCK	O	Viterbi lock indicator
58	DLOCK	O	Demodulator lock indicator
59	V_{DDD8}	–	digital supply voltage 8 (core and input periphery)
60	V_{DDD9}	–	digital supply voltage 9 (core and input periphery)
61	TEST	I	test pin (normally connected to ground)
62	TRST	I	BST optional asynchronous reset (normally connected to ground)
63	TCK	I	BST dedicated test clock (normally connected to ground)
64	SCLT	O	serial clock of I^2C-bus loop-through
65	SDAT	I/O	serial data of I^2C-bus loop-through
66	V_{DDD10}	–	digital supply voltage 10 (core and input periphery)
67	V_{SSD11}	–	digital ground 11 (output periphery)
68	V_{SSD12}	–	digital ground 12 (core and input periphery)
69	TMS	I	BST input control signal (normally connected to ground)
70	TDO	O	BST serial test data out
71	TDI	I	BST serial test data in (normally connected to ground)
72	V_{DDD11}	–	digital supply voltage 11 (core and input periphery)
73	V_{SSD13}	–	digital ground 13 (core and input periphery)
74	$V_{SSD(AD)}$	–	digital ground A/D converter
75	$V_{DDD(AD)}$	–	digital supply A/D converter
76	$V_{ref(B)}$	O	bottom reference voltage for ADC
77	V_{SSA1}	–	analog ground 1
78	QA	I	analog input Q
79	$V_{ref(Q)}$	O	AGC decoupling - Q path

●**Pin Function (3/3)**

PIN	SYMBOL	I/O	DESCRIPTION
80	IA	I	analog input I
81	V_{SSA2}	–	analog ground 2
82	$V_{ref(I)}$	O	AGC decoupling - Ipath
83	V_{DDA}	–	analog supply voltage
84	V_{DDXTAL}	–	supply voltage for crystal oscillator
85	XTALI	I	crystal oscillator input
86	XTALO	O	crystal oscillator output
87	V_{SSXTAL}	–	ground for crystal oscillator
88	V_{DDD12}	–	digital supply voltage 12 (core and input periphery)
89	V_{DDD13}	–	digital supply voltage 13 (core and input periphery)
90	V_{SSD14}	–	digital ground 14 (core and input periphery)
91	DiSCTRL	O	22 kHz / 44kHz output for dish control applications
92	V_{SSD15}	–	digital ground 15 (output periphery)
93	V_{SSD16}	–	digital ground 16 (core and input periphery)
94	V_{AGC}	O	Tuner AGC output
95	n.c.	–	not connected
96	V_{DDD14}	–	digital supply voltage 14 (output periphery)
97	V_{DDD15}	–	digital supply voltage 15 (core and input periphery)
98	OUTSD	O	Sigma Delta Output
99	I0	I	digital I-input bit 0 (ADC bypass - LSB)
100	I1	I	digital I-input bit 1 (ADC bypass)

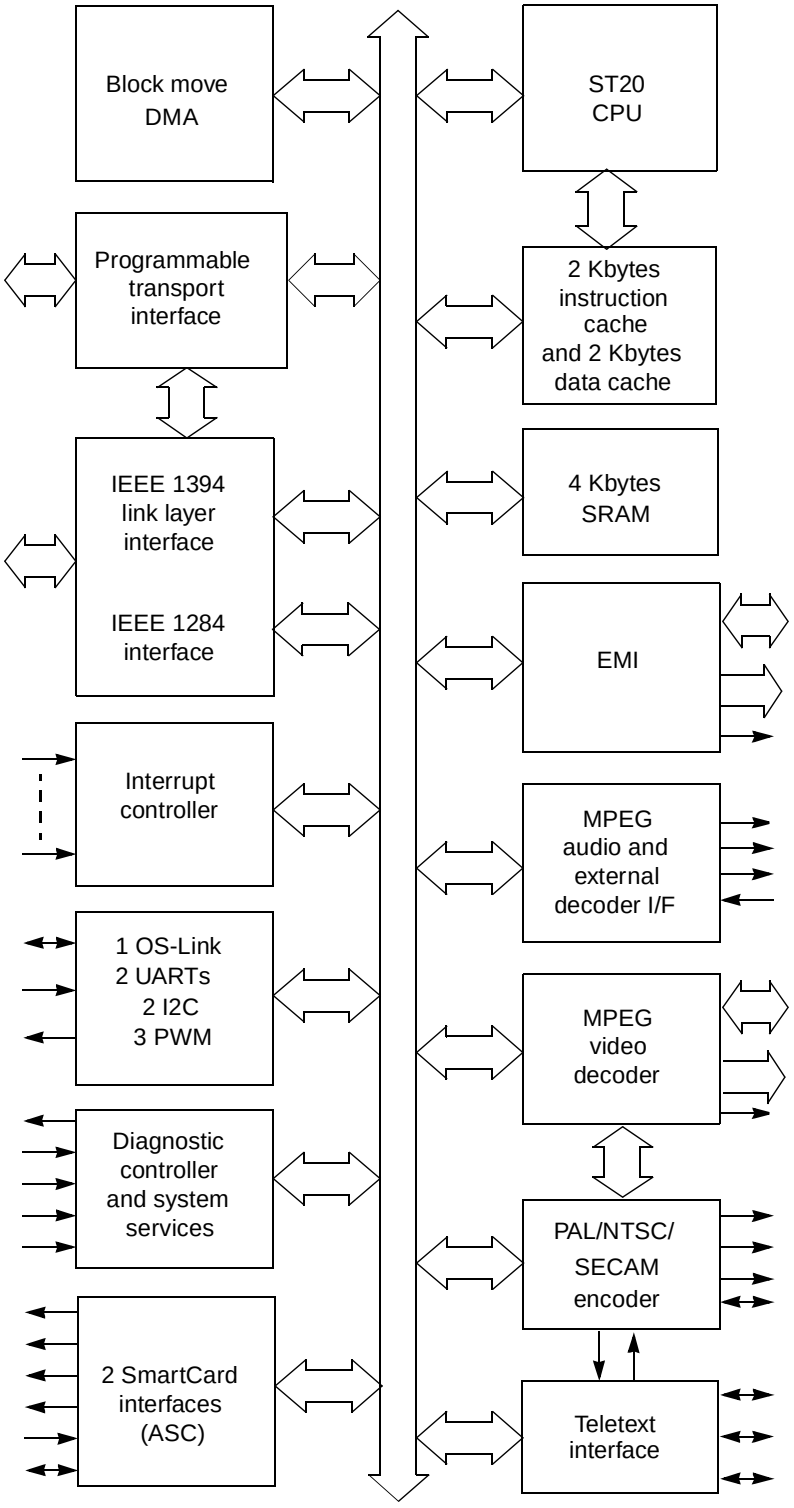
Note

1. Pins I0 to I6, Q0 to Q6, SCL, SDA, $\overline{INT}$, SCLT, SDAT, V_{AGC} and OUTSD are 5V tolerant.
2. The structure of I/O's and the maximum output drive are specified in Section 12

■ STI5512MWD (MAIN ASSY(2/7) : IC2001)

• **Programmable Transport IC**

●**Block Diagram**



●Pin Function (1/5)

Signal names are prefixed by **not** if they are active low; otherwise they are active high.

Pin	Number	Function
VDD	13	Power supply
GND	16	Ground
VClamp1-3[1]	3	Power supply for clamp diodes
VDDA0-1	2	Analog power supply for PAL/NTSC/SECAM encoder
VSSA0-1	2	Analog ground for PAL/NTSC/SECAM encoder
RTCVDD	1	Real time clock supply
VDD_VPLL	1	Analog power supply for video PLL
VSS_VPLL	1	Analog ground for video PLL

Table 1 Power supply pins

1. The VClamp pins are a power supply bus used to diode clamp the voltage on 5V tolerant digital input or output pins to. The voltage on the digital signal pin is then clamped to within VImax (5.5V) if the applied voltage is increased above 5V.

If the device is to be interfaced to 3.3V logic signals only, then the VClamp pins can be connected to the STi5512 3.3V VDD power supply. However if any pin is to be interfaced to a 5V logic signal, then the VClamp pins must be connected to the 5V power supply (the 5V logic device power supply). Note in this case the 5V power supply must be capable of sinking the clamp current of transient signals above 5V.

In the latter case it is important to ensure the correct power supply ramp sequence. The VClamp power supply must be applied before or at the same time as the VDD 3.3V power supply. This is to ensure that during power supply power up and power down, VClamp > VDD + 0.5V.

Pin	In/Out	Function
R_OUT[1]	out	Red output
G_OUT[1]	out	Green output
B_OUT2[1]	out	Blue output
C_OUT[1]	out	Chroma output
CV_OUT[1]	out	Composite video output
Y_OUT[1]	out	Luma output
I_REF_DAC_RGB[1]	in	DAC current reference
I_REF_DAC_YCC[1]	in	DAC current reference
V_REF_DAC_RGB[1]	in	DAC voltage reference
V_REF_DAC_YCC[1]	in	DAC voltage reference
OSD_ENABLE	in/out	OSD enable
notHSYNC	in/out	Horizontal sync
ODD_OR_EVEN	in/out	Vertical sync
YC0-7[2]	output	Digital YUV output
CFC	input	DENC color burst phase and frequency control. This pin can be used in non-scart based Genlock applications. If it is not used, this pin must ground.

Table 2 Video output interface pins

●Pin Function (2/5)

1. The digital encoder video outputs are analogue signals and are not 5V tolerant. The same applies to the video DAC voltage and current reference pins.

2. The **YC0** pin is tri-stated during reset and then sampled at the end of the reset to determine whether the EMI pins are in STi5510 or STi5512 mode. If the **YC0** pin is sampled high (i.e at VDD) then the STi5510 mode is selected for the EMI pins and a low value selects STi5512 mode. In STi5512 mode the address shift for bank 3 is dependent on the boot bank width and the strobe pins are tri-stated when the EMI bus is granted to an external DMA device. External 10KΩ pull-up or pull-down resistors should be fitted to the **YC0** according to the functionality desired. If this pin is left *not* connected, the pin will be pulled high by an internal pull-up and will default the EMI pins to STi5510 mode.

Pin	In/Out	Function
SCLK/A_C_STB	out	Serial clock or AC-3 data strobe
PCM_DATA/A_C_DATA	out	PCM data out or AC-3 data out
PCMCLK	in/out	PCM clock
LRCLK/A-WORD_CLK	out	Left/right clock or AC-3 word clock
notA_C_REQ i	n	AC-3 data request
notA_PTS_STB	in	AC-3 audio PTS strobe

Table 3 AC-3/MPEG1 audio output interface pins

Pin	In/Out	Function
Interrupt0-1	in	Interrupt

Table 4 External interrupt pins

Pin	In/Out	Function
ClockIn	in	System input clock - PLL or TimesOneMode
SpeedSelect0-1	in	PLL speed selector
notRST	in	System reset
CPUAnalyse / TrigIn	in	Error analysis / External trigger input to DCU
CPUReset	in	Soft reset for analyzing from OS-Link
ErrorOut / TrigOut[1]	in/out, out	Error indicator / Signal to trigger external debug circuitry (e.g. LSA)

Table 5 System services pins

1. This pin is tri-stated during reset and then sampled at the end of the reset to determine whether the OS-Link is active and to determine the function of the shared **CPUAnalyse / TrigIn** and the **ErrorOut / TrigOut**, as described in the *System Services* chapter. If the **ErrorOut** pin is sampled high (i.e at VDD) then the DCU signals (**TrigIn** and **TrigOut**) are selected and a low value indicates OS-Link signals (i.e. **CPUAnalyse**, **ErrorOut**) are to be used. External 10KΩ pull-up or pull-down resistors should be fitted to the **ErrorOut** according to the functionality desired.

●Pin Function (3/5)

Pin	In/Out	Function
MemAddr2-23 out		Address bus
MemData0-31	in/out	Data bus. **MemData0** is the least significant bit (LSB) and **MemData31** is the most significant bit (MSB).
MemRdnotWr out		ReadnotWrite strobe
MemReq	in	Direct memory access request
MemGrant	out	Direct memory access granted
MemWait i	n	Memory cycle extender
notMemCAS0,2	out	CAS strobes for SDRAM/DRAM in Banks 0 and 1
notMemCAS1	out	CAS strobe for DRAM or SDRAM clock
notMemCAS3	out	CAS strobe for DRAM or sub-bank chip select for bank 3
notMemRAS0	out	RAS strobe for SDRAM/DRAM in Bank 0, chip select for Bank0 or RAS strobe for lowest DRAM sub-bank in Bank0
notMemRAS1	out	RAS strobe for highest DRAM sub-bank in Bank0 or SDRAM Chip select signal for highest sub-bank of Bank0
notMemRAS2	out	RAS strobe for SDRAM/DRAM in bank 1, chip select for Bank1 or RAS strobe for lowest DRAM sub-bank in Bank1
notMemRAS3	out	RAS strobe for highest DRAM sub-bank in Bank1 or SDRAM Chip select signal for Bank1
notMemCSROM	out	Chip select strobe for ROM in bank3.
notSDRAMCS0	out	SDRAM Chip select signal for Bank0 or lowest sub-bank of Bank0
notMemOE	out	Output enable strobe - banks 0-3.
notMemBE0-3	out	Byte enable strobes - banks 0-3.
notMemCS2	out	Chip select strobe for memory in bank 2.
BootSource0-1	in	Boot from ROM or from link.
ProcClockOut	out	Processor clock.

Table 6 STi5512 External memory interface pins

Pin	In/Out	Function
AD0-12 out		SDRAM address bus
DQ0-15	in/out	SDRAM data bus (lower byte)
notSDCS0	out	SDRAM chip select for first SDRAM
notSDCS1/AD13	out	SDRAM chip select for second SDRAM or AD13
notSDCAS out		SDRAM CAS
notSDRAS out		SDRAM RAS
notSDWE out		SDRAM write enable
MEMCLKIN	in	SDRAM memory clock input
MEMCLKOUT	out	SDRAM memory clock output
DQML	out	DQ mask enable (lower)
DQMU	out	DQ mask enable (upper)

Table 7 Shared SDRAM interface pins

●Pin Function (4/5)

Pin	In/Out	Function
LPClockIn[1]	in	Low power input clock
LPClockOsc[1]	in/out	Low power clock oscillator
AUX_CLK_OUT	out	Auxiliary clock for general use

Table 8 Low power controller and real time clock pins

1. The low power clock pins are not 5V tolerant.

Pin	In/Out	Function
PIO0[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO1[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO2[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO3[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO4[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)

Table 9 PIO pins

Pin	In/Out	Function
LinkIn	in	Serial data input channel
LinkOut	out	Serial data output channel

Table 10 OS-Link pins

Pin	In/Out	Function
TSInByteClk	in	Link IC byte clock
TSInByteClkValid	in	Link IC byte clock valid edge
TSInData0-7	in	Link IC data
TSInError	in	Link IC packet error
TSInPacketClk	in	Link IC packet strobe

Table 11 Transport stream input pins

Pin	In/Out	Function
TtxtEvennotOdd	in	Teletext even not odd vertical sync signal
TtxtHsync	in	The HSYNC signal input when the teletext interface is operating in the input mode

Table 12 Teletext interface

●Pin Function (5/5)

The teletext clock and data inputs are shared PIO pins, as shown in Table 15 .

High speed data port pins have a dual function, and can be used either to interface to an external IEEE 1394 link layer controller or provide an IEEE 1284 parallel port interface.

Pin	In/Out	Function
1284Data0-7 / AVData0-7	in/out	IEEE 1284 port data or AV data
1284notSelectIn	in	IEEE 1284 port control signals or AV signals
1284notInit / AVPacketTag3	in	
1284notFault / AVPacketTag2	out	
1284notAutoFd / AVPacketTag1	in	
1284Select / AVPacketTag0	out	
1284PError / AVByteClkValid	out, in/out	
1284Busy / AVPacketClk	out, in/out	
1284notAck / AVByteClk	out	
1284notStrobe/AVPacketError	in	

Table 13 High-speed data port pins

Pin	In/Out	Function
TDI	in	Test data input
TDO	out	Test data output
TMS	in	Test mode select
TCK	in	Test clock
notTRST	in	Test logic reset

Table 14 TAP pins

● PIO pins and alternative functions

To improve flexibility and to allow the STi5512 to fit into different set-top box application architectures, the input and output signals from some of the peripherals are not directly connected to the pins of the device. Instead they are assigned to the alternative function inputs and outputs of a PIO port bit. This scheme allows these pins to be configured as general purpose PIO if the associated peripheral input or output is not required in that particular application.

Table 17 shows the assignment of the alternative functions to the PIO bits. Parentheses ( ) in the table indicate suggested or possible pin usages as a PIO, not an alternative function connection.

Port bit	Alternative function of PIO pins				
	PIO port 0	PIO port 1	PIO port 2	PIO port 3	PIO port 4
0	ASC0TxD or Sc1DataOut	SSC0 MTSR	ASC2TxD or Sc0DataOut	SSC1 MTSR	ASC3TxD
1	ASC0TRxD or Sc1DataIn	SSC0 MRST	ASC2RxD or Sc0DataIn	SSC1 MRST	ASC3RxD
2	Sc1ClkGenExtClk	SSC0 SClk	Sc0ClkGenExtClk	SSC1 SClk	TtxtClockIn
3	Sc1Clk	PWMOut0	Sc0Clk	CaptureIn0	1284PeriphLogicH/ASC3 CTS
4	(Sc1RST)	PWMOut1	(Sc0RST)	CaptureIn1	1284HostLogicH/ASC3 RTS
5	(Sc1CmdVcc)	ASC1TxD	(Sc0CmdVcc)	CaptureIn2	Interrupt2
6	(Sc1CmdVpp) Sc1Dir	ASC1RxD	(Sc0CmdVpp) Sc2Dir	CompareOut2	Interrupt3
7	(Sc1Detect)	PWMOut2	(Sc0Detect)	1284InnotOut	TtxtData

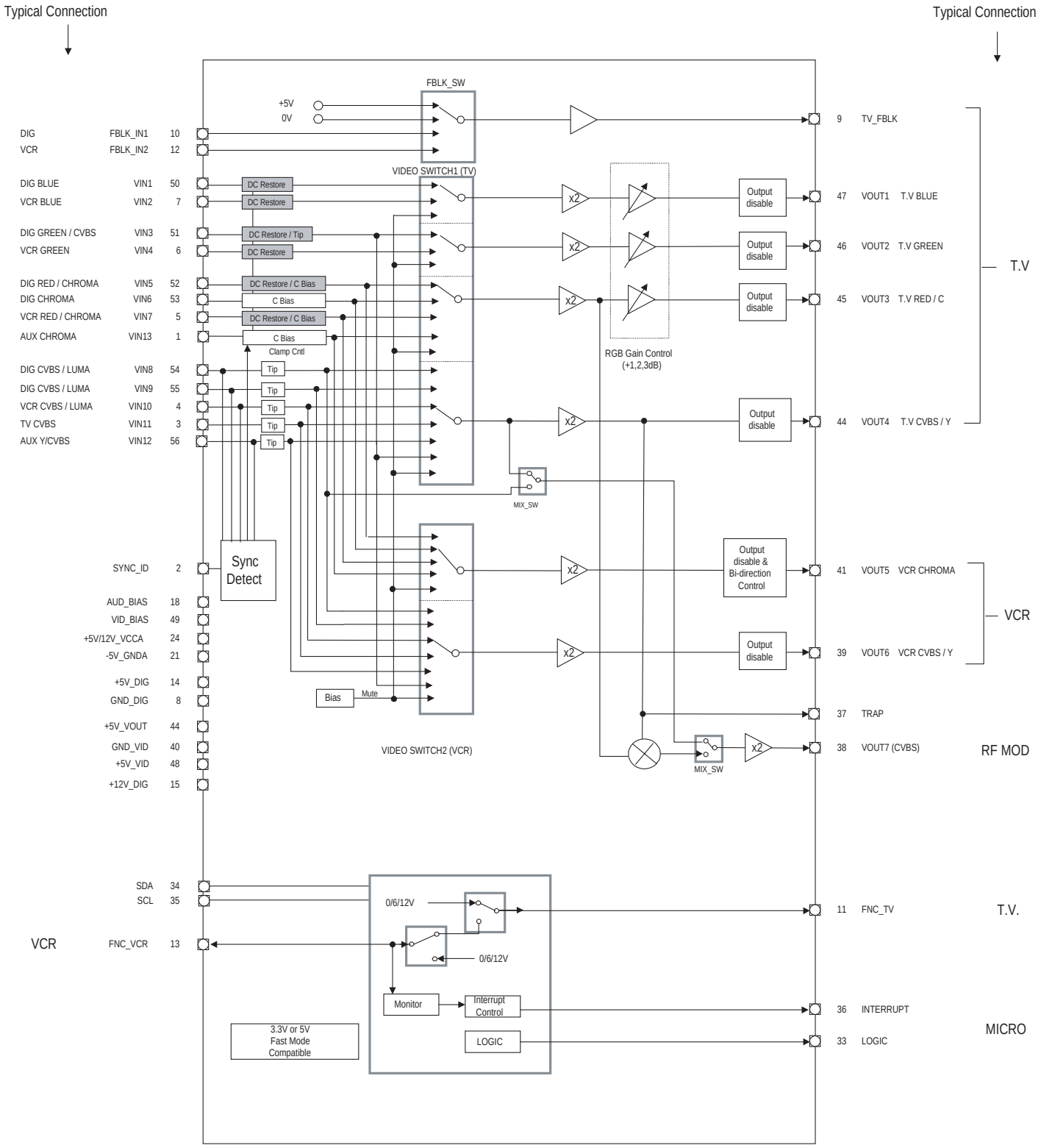
Table 15 Alternative function of PIO pins

■ CXA2161R (MAIN ASSY(4/7) : IC4001)

- **AV Switch**

●Block Diagram(1/2)

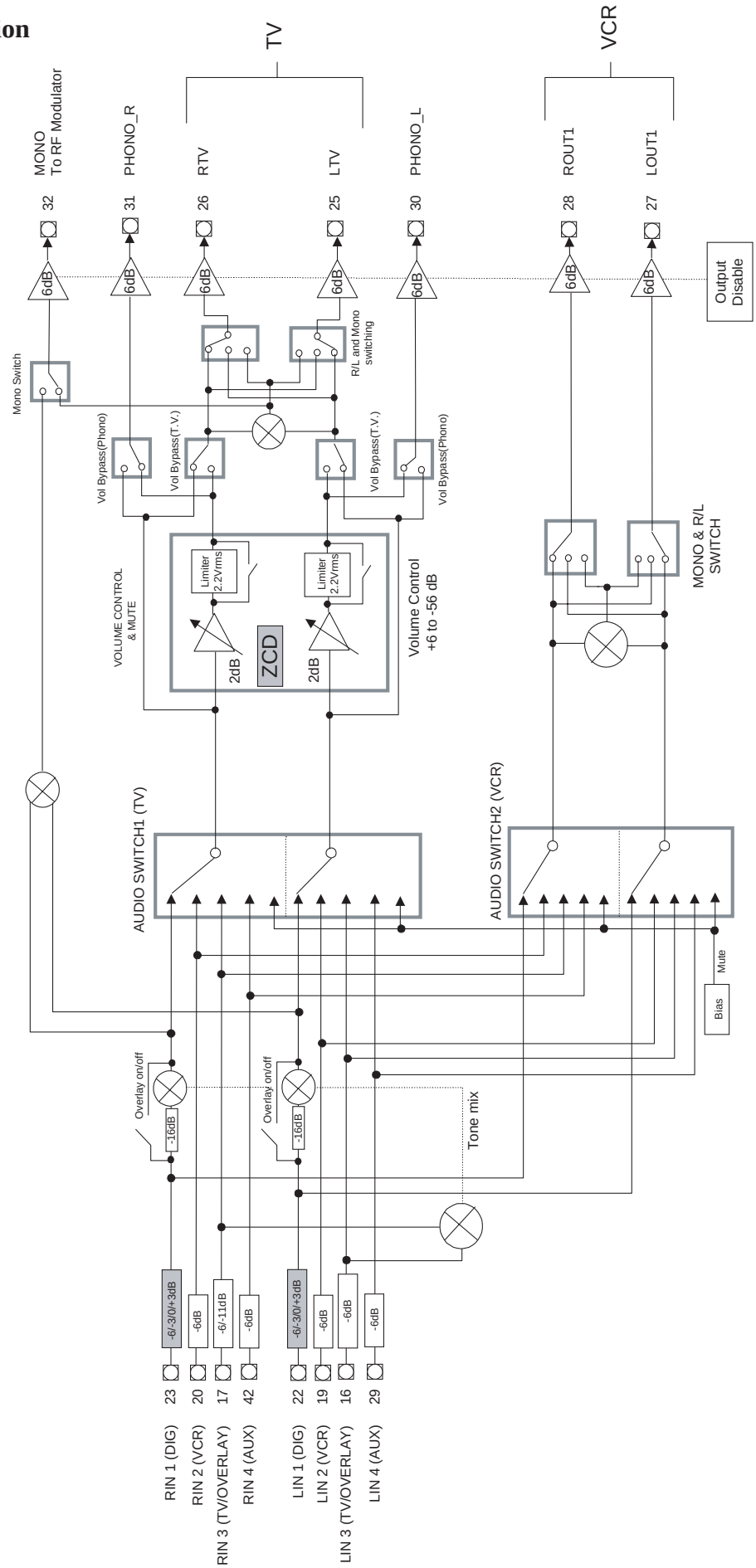
Video and Digital section



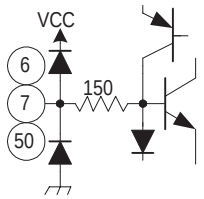
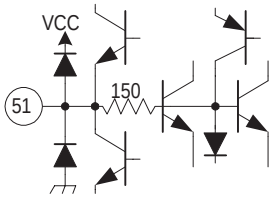
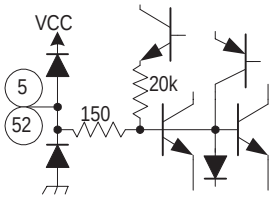
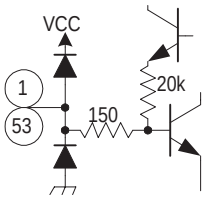
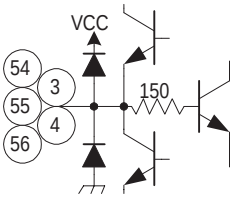
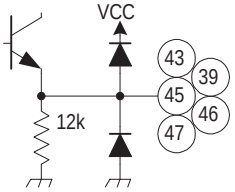
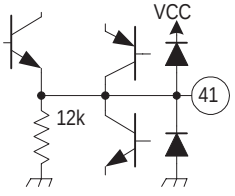
Note: All video outputs contain 75Ω drivers, except Vout7.

●Block Diagram(2/2)

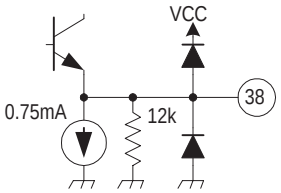
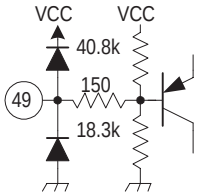
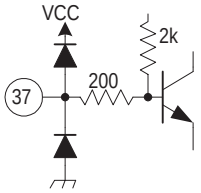
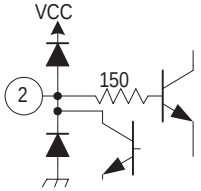
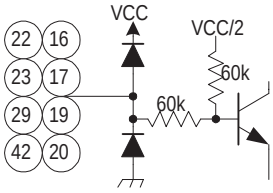
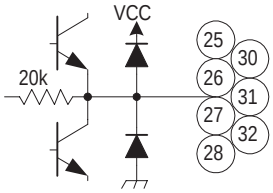
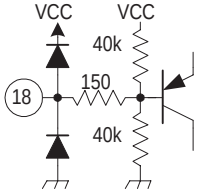
Audio section



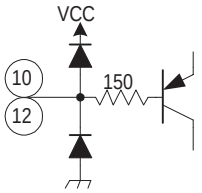
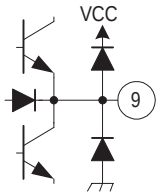
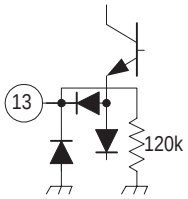
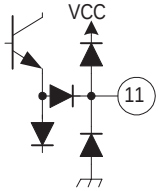
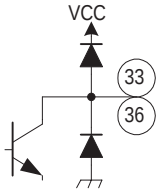
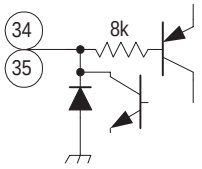
●**Pin Function (1/3)**

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description
50 7 6	VIN_1 VIN_2 VIN_4	2.4		RGB signal inputs
51	VIN_3	2.4 2.35		RGB signal input OR CVBS signal input
52 5	VIN_5 VIN_7	2.4 3.0		RGB signal inputs OR Chrominance signal inputs
53 1	VIN_6 VIN_13	3.0		Chrominance signal inputs
54 55 4 3 56	VIN_8 VIN_9 VIN_10 VIN_11 VIN_12	2.35		CVBS / Luminance signal inputs
47 46 45 43 39	VOUT_1 VOUT_2 VOUT_3 VOUT_4 VOUT_6	0.4		RGB / CVBS signal outputs
41	VOUT_5	0.4		Chrominance signal output

●Pin Function (2/3)

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description	
38	VOUT_7	0.4		Typically RF modulator signal output Minimum load = 20k resistive	
49	VID_BIAS	0.9		Internal reference bias for video circuits. A capacitor is connected from this pin to GND. Typically 100nF	
37	TRAP	2.3		Connects trap circuit for subcarrier	
2	SYNC_ID	2.5		Sync detect circuit time constant, resistor and capacitor connection pin	
22 23 19 20 16 17 29 42	LIN_1 RIN_1 LIN_2 RIN_2 LIN_3 RIN_3 LIN_4 RIN_4	6.0 (Single) 0.0 (Dual)		Audio signal inputs	
25 26 27 28 30 31 32	LTV RTV LOUT1 ROUT1 PHONO_L PHONO_R MONO	6.0 (Single) 0.0 (Dual)		Audio signal outputs	
18	AUD_BIAS	6.0 (Single) 0.0 (Dual)		Internal reference bias for audio circuits.	Capacitor connected to GND. (Typically 22µF) Connected directly to GND.

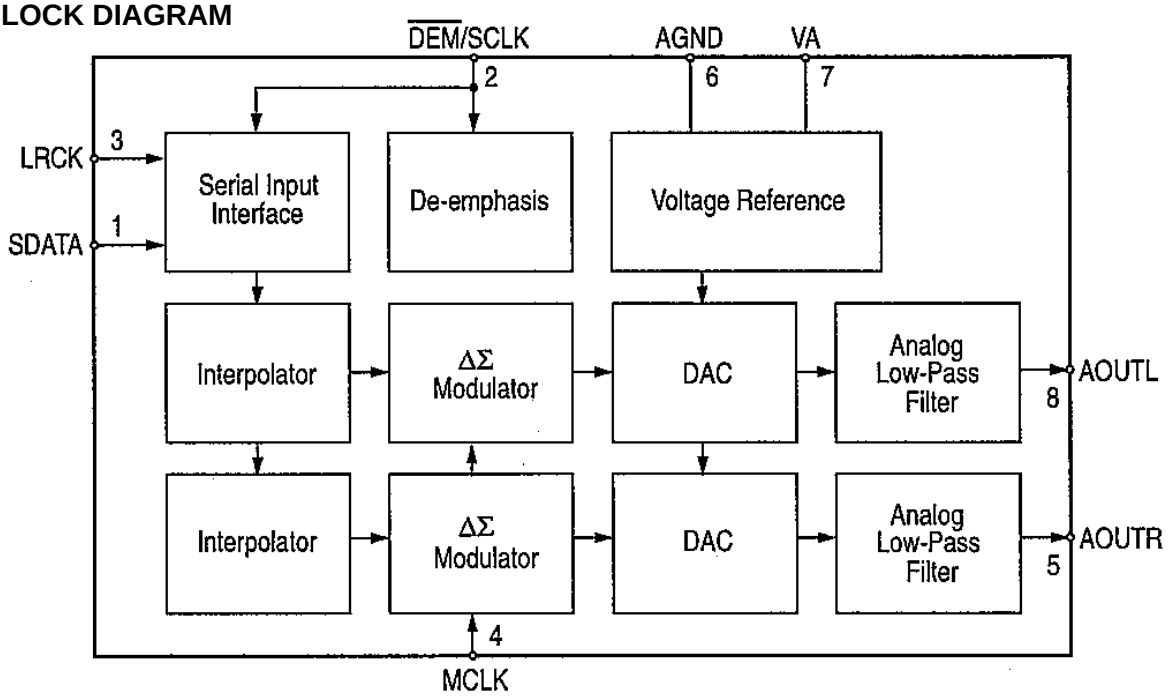
●**Pin Function (3/3)**

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description
10 12	FBLK_IN1 FBLK_IN2	-		Fast blanking signal inputs
9	TV_FBLK	-		Fast blanking signal output
13	FNC_VCR	-		SCART function pin 8 input / output to VCR
11	FNC_TV	-		SCART function pin 8 output to TV
33	LOGIC	-		Open collector logic outputs Typically connect to +5V through 10k resistor.
36	INTRUPT	-		
35	SCL	-		I^2C bus clock line
34	SDA			I^2C bus data line
14	+5V_DIG	5.0		Digital supply
44	+5V_VOUT			Video output supply
48	+5V_VID			Video supply
15	+12V_DIG	12.0		Digital supply
21	-5V_GNDA	-5.0 / 0.0		Audio supply / ground
24	+5V/12V_VCCA	5.0 / 12.0		Audio supply
8	GND_DIG	0.0		Digital ground
40	GND_VID	0.0		Video ground

■ CS4335-KS (MAIN ASSY(4/7) : IC4002)

• **DAC**

● BLOCK DIAGRAM



● PIN DESCRIPTIONS

SERIAL DATA INPUT	**SDATA**	1	8	**AOUTL**	ANALOG LEFT CHANNEL OUTPUT
DE-EMPHASIS / SCLK	**DEM/SCLK**	2	7	**VA**	ANALOG POWER
LEFT / RIGHT CLOCK	**LRCK**	3	6	**AGND**	ANALOG GROUND
MASTER CLOCK	**MCLK**	4	5	**AOUTR**	ANALOG RIGHT CHANNEL OUTPUT

Power Supply Connections

VA - Analog Power, PIN 7

Analog supply. Nominally +5V.

AGND - Analog Ground, PIN 6

Analog ground reference.

Analog Outputs

AOUTL - Analog Left Cannel Output, PIN 8

Analog output for the left channel. Typically 3.5V Vpp for a full-scale input signal.

AOUTR - Analog Right Cannel Output, PIN 5

Analog output for the right channel. Typically 3.5V Vpp for a full-scale input signal.

Digital Inputs

MCLK - Master Clock Input, PIN 4

The frequency must be 256x, 384x or 512x the input sample rate in Base Rate Mode (BRM) and either 128x or 192x the input sample rate in High Rate mode (HRM).

LRCK - Left/Right Clock, PIN 3

This input determine which channel is currently being input on the Audio Serial Data Input pin, SDATA.

SDATA - Audio Serial Data Input, PIN 1

Two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4335 via internal or external SCLK and the channel is determined by LRCK.

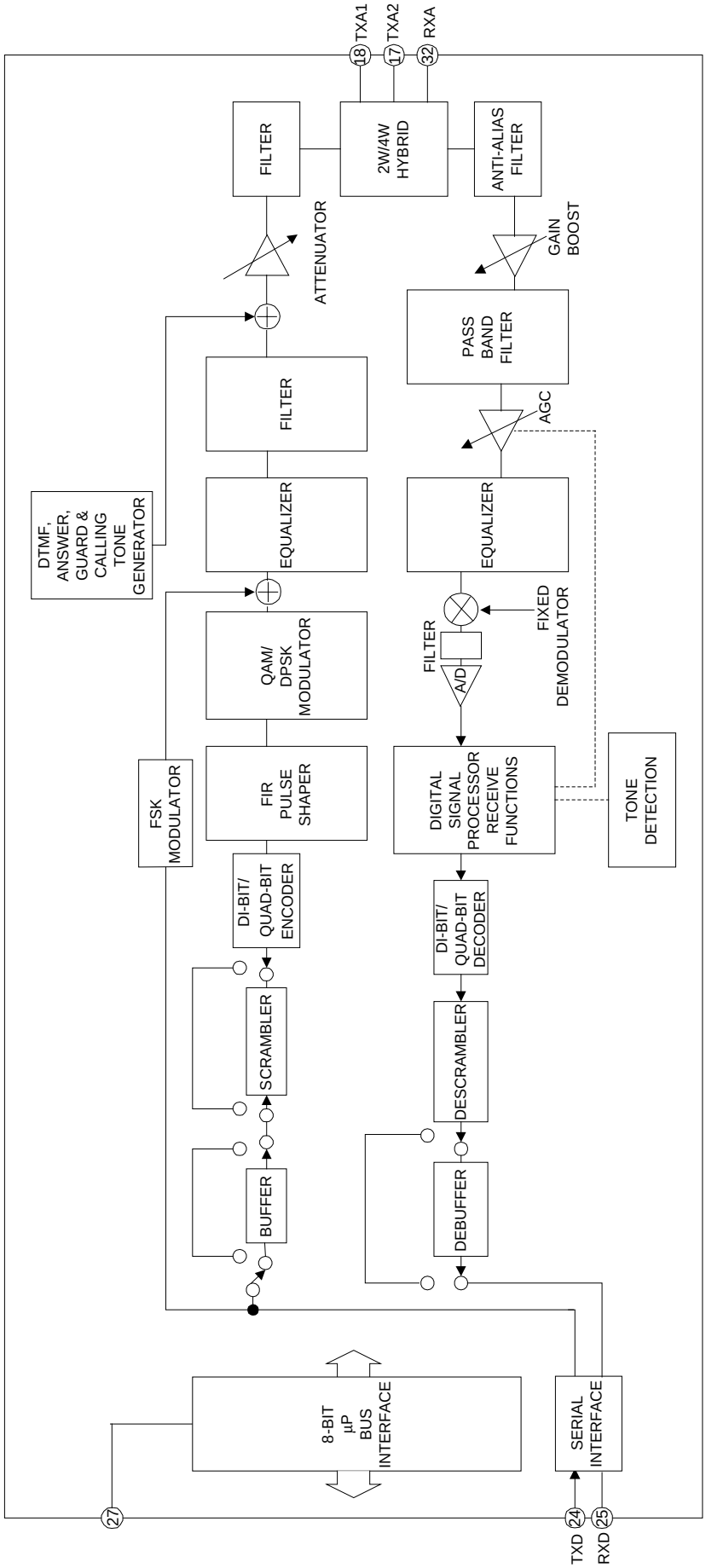
$\overline{\text{DEM}}$/SCLK - De-emphasis / External serial clock input, PIN 2

A dual-purpose input used for de-emphasis filter control or external serial clock input.

73K324BL-IH (MAIN ASSY(6/7) : IC6005)

- **Modem IC**

●Block Diagram



●Pin Function (1/3)

POWER

NAME	PIN	TYPE	DESCRIPTION
GND	1	I	System ground
VDD	16	I	Power supply input, 5 V ±10% (73K324BL). Bypass with 0.1 and 22 μF capacitors to GND.
VREF	31	O	An internally generated reference voltage. Bypass with 0.1 μF capacitor to ground.
ISET	28	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 μF capacitor.

PARALLEL MICROPROCESSOR CONTROL INTERFACE MODE

ALE	13	I	ADDRESS LATCH ENABLE: The falling edge of ALE latches the address on AD0-AD2 and the chip select on &6 .
AD0-AD7	5-12	I/O	ADDRESS/DATA BUS: These bi-directional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	23	I	CHIP SELECT: A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	2	O	OUTPUT CLOCK: This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 times the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	20	O	INTERRUPT: This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	15	I	READ: A low requests a read of the 73K324BL internal registers. Data can not be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	30	I	RESET: An active high signal on this pin will put the chip into an inactive state. All Control Register bits (CR0, CR1, tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on-reset using a capacitor to VDD.

●**Pin Function (2/3)**

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	PIN	TYPE	DESCRIPTION
$\overline{WR}$	14	I	WRITE: A low on this informs the 73K324BL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR CONTROL INTERFACE MODE

NAME	PIN	TYPE	DESCRIPTION
AD0-AD2	5-7	I	REGISTER ADDRESS SELECTION: These lines carry register addresses and should be valid during any read or write operation.
DATA (AD7)	12	I/O	SERIAL CONTROL DATA: Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	15	I	READ: A low on this input informs the 73K324BL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	14	I	WRITE: A low on this input informs the 73K324BL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

NOTE: The serial control mode is provided by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become the register address.

●**Pin Function (3/3)**

DTE USER

NAME	PIN	TYPE	DESCRIPTION
EXCLK	22	I	EXTERNAL CLOCK: This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	26	O	RECEIVE CLOCK: The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	25	O	RECEIVED DATA OUTPUT: Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	21	O	TRANSMIT CLOCK: This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In internal mode the clock is generated internally. In external mode TXCLK is phase locked to the EXCLK pin. In slave mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	24	I	TRANSMIT DATA INPUT: Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bps or 300/1200 baud) no clocking is necessary. DPSK data must be 1200/600 bps +1%, -2.5% or +2.3%, -2.5 % in extended over speed mode.

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ANALOG INTERFACE AND OSCILLATOR

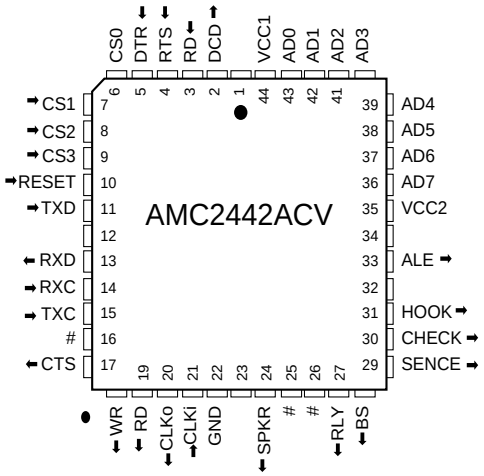
NAME	PIN	TYPE	DESCRIPTION
RXA	32	I	Received modulated analog signal input from the telephone line interface.
TXA1 / TXA 2	18 / 17	O	(differential) Transmit Analog. These pins provide the analog output signals to be transmitted to the telephone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
XTL1 / XTL2	3 / 4	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to ground. XTL2 can also be driven from an external clock.
$\overline{OH}$	27	O	OFF-HOOK RELAY DRIVER: This signal is an open drain output capable of sinking 40 mA and is used for controlling a relay. The output is the complement of the OH register bit in the ID Register.

AMC2442ACVF(0.87) (MAIN ASSY(6/7) : IC6006)

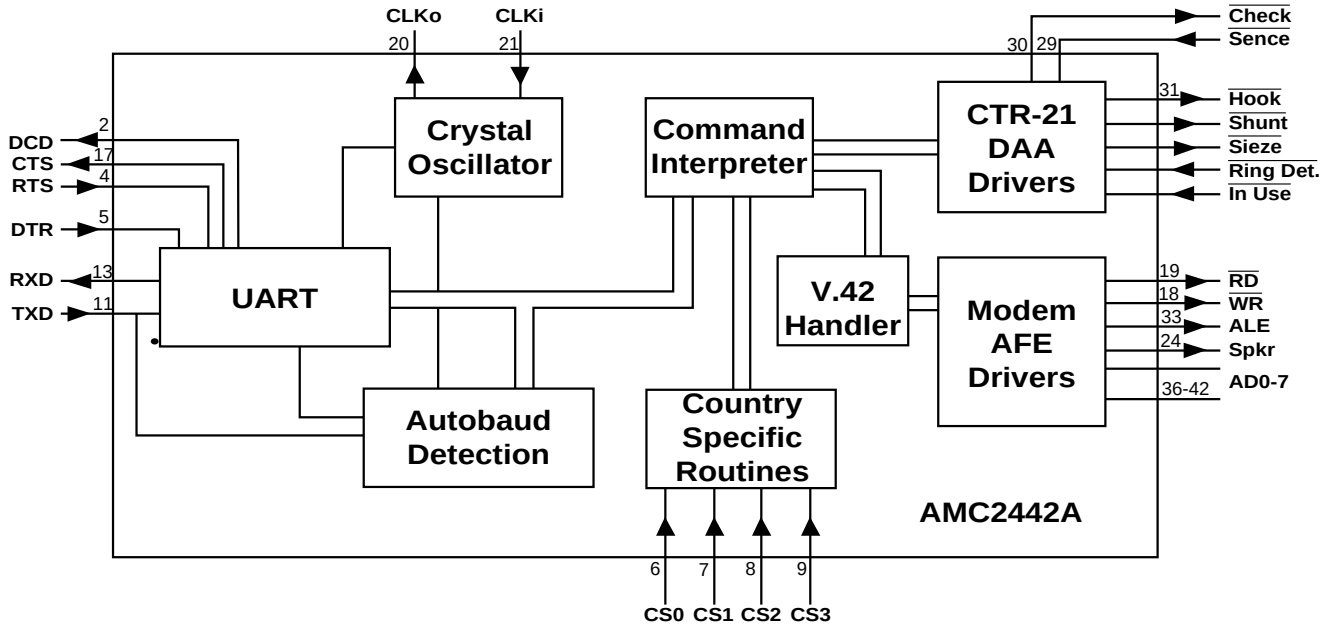
- **Modem Controller**

●Pinouts/Blockdiagram

Pinouts



BLOCK DIAGRAM



●Pin Function

PIN NUMBER	Pin Name	I/O TYPE	Description
2	DCD	Output	DTE Data Carrier Detect output signal. Indicates modem has detected carrier.
3	RING	Input	Ring detector input. This pin assumes that a half wave opto coupler is used in the telephone line DAA circuit in the frequency detection algorithm.
4	RTS	Input	DTE Ready To Send input signal. Used for hardware flow control.
5	DTR	Input	DTE Data Terminal Ready input signal. Used to enable modem device
6	CS0	Intput	Country Selection bit 0 (Internal pull up)
7	CS1	Input	Country Selection bit 1 (Internal pull up)
8	CS2	Input	Country Selection bit 2 (Internal pull up)
9	CS3	Input	Country Selection bit 3 (Internal pull up)
10	RESET	Input	Reset signal to the AMC2442A Controller. Active High.
11	TXD	Input	DTE Transmit Data Pin. All data communication from the DTE connects via this pin.
13	RXD	Output	DTE Receive Data Pin. All data communication to the DTE connects via this pin.
14	RXC	Input	Receiver Clock Input from AFE. Used in PSK, QAM and synchronous data mode.
15	TXC	Input	Transmitter Clock Input from AFE. Used in PSK, QAM and synchronous data mode.
16	Free	I/O	DO NOT CONNECT
17	CTS	Output	DTE Clear To Send output signal. Used for hardware flow control.
18	WR	Output	Write signal to AFE. Goes active low whenever the SMC wishes to write to the AFE
19	RD	Output	Read signal to AFE. Goes active low whenever the SMC wishes to read from the AFE
20	CLKo	Output	Buffered Clock output signal. Also used as a crystal drive signal when required.
21	CLKi	Input	Clock input signal. The SMC requires an 11.0592MHz signal on this pin.
22	GND	Power	Controller Ground connection
24	SPKR	Output	Speaker Enable drive
25	Free	I/O	DO NOT CONNECT
26	Free	I/O	DO NOT CONNECT
27	RLY	Output	DAA Line Seize relay control. Used if DPCO relay is used to share the telephone with a standard telephone instrument.
28	BS	Output	DAA Bell Shunt control. Used during LD dialling to provide a low impedance loop.
29	SENSE	Input	Line-In-Use detection input.
30	CHECK	Output	Line-In-Use circuit drive pin.
31	HOOK	Output	DAA Hook switch control. Delayed from Seize to allow for a low cost opto coupler.
32	NC	I/O	DO NOT CONNECT
33	LATCH	Output	ALE signal to AFE. Goes active high to latch an address into the AFE
35	VCC2	Power	Auxiliary power supply pin.
36->43	AD7->AD0	I/O	Multiplex Address / Data bus connections to AFE.
44	VCC1	Power	Main power supply pin.
1	NC	I/O	DO NOT CONNECT
12	NC	I/O	DO NOT CONNECT
23	NC	I/O	DO NOT CONNECT
34	NC	I/O	DO NOT CONNECT

■ PE5181A (MAIN ASSY(7/7) : IC7001)

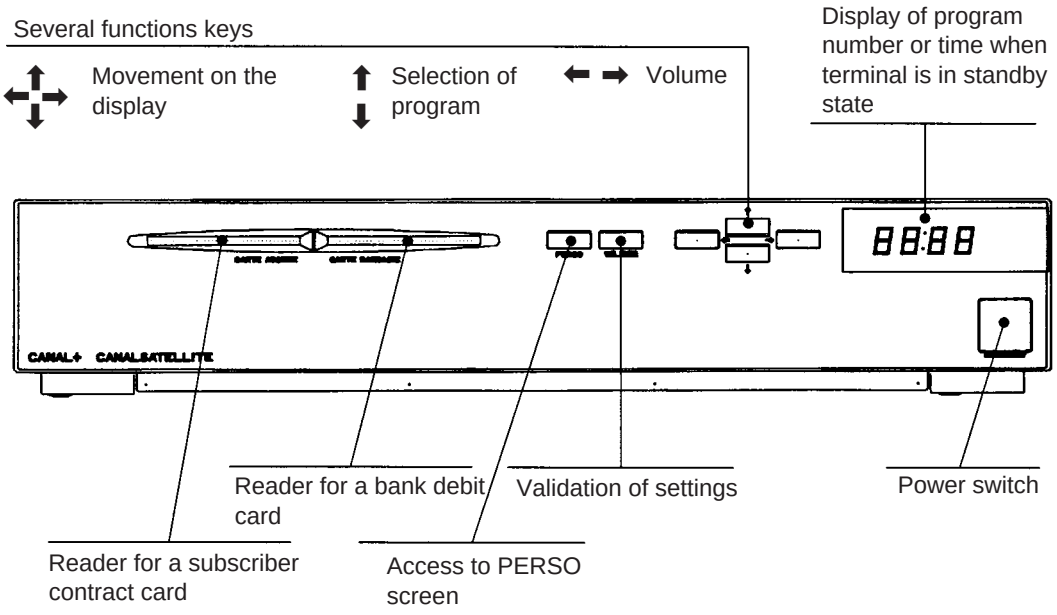
• **Sub CPU**

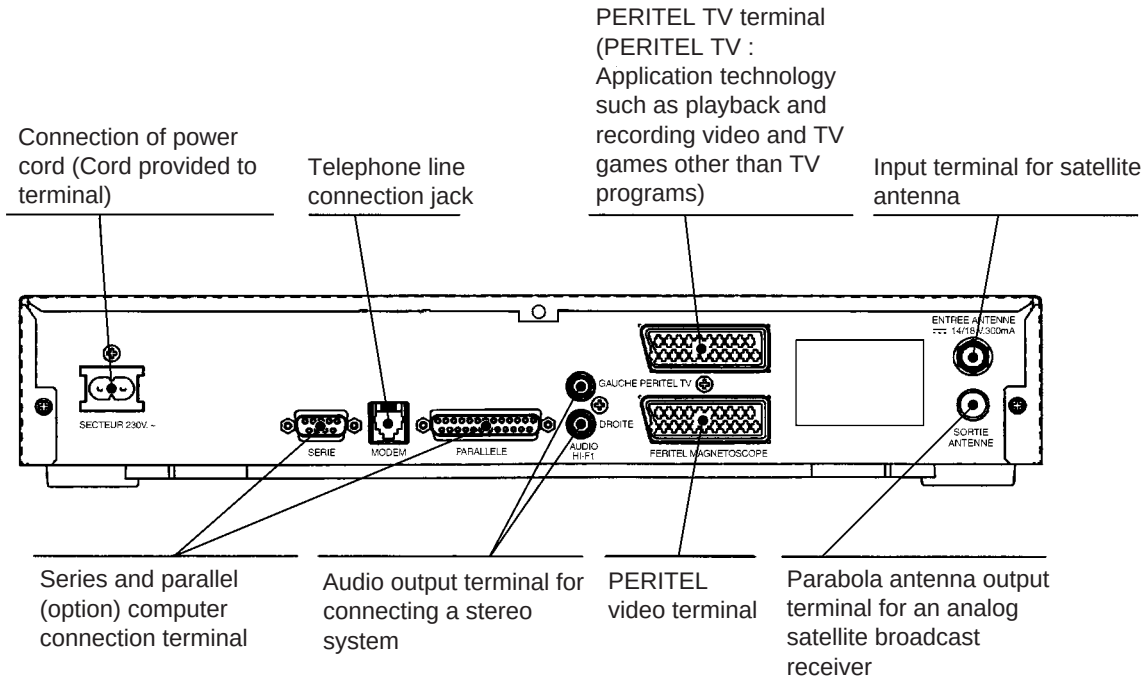
●**Pin Function**

No.	Mark	Pin Name	I/O	Active	Pin Function
1	P50	LED10	O	Low	Front LED, seg
2	P51	LED11	O	Low	Front LED, seg
3	P52	LED12	O	Low	Front LED, seg
4	P53	LED13	O	Low	Front LED, seg
5	P54	LED14	O	Low	Front LED, seg
6	P55	LED15	O	Low	Front LED, seg
7	P56	LED16	O	Low	Front LED, seg
8	P57	LED17	O	Low	Front LED, seg
11	P30	IRQ_TEIDEN	O	Low	Power failure interruption (L output only at power failure)
12	P31	IRQ_KEY	O	Low	Remote controller / key interruption
13	SDA0	I2C_SDA	O		I2C_SDA Output
14	SCL0	I2C_SCL	I		I2C_SCL Input
15	P34	×	O		
16	P35	×	O		
17	P36	×	O		
18	P20	×	O		
19	P21	×	O		
20	P22	×	O		
21	P23	×	O		
22	P24	×	O		
23	P25	SUB_MUTE	O	Low	Power_off Mute
26	P17	TEST	I	Low	For production line
27	P16	RC_MM	I	Any	RC_MM Selection (H : Disabel, L : Enable)
28	P15	pioneer/philips	I	Any	Remote control code selection (H : Philips, L : Pioneer)
29	P14	XHALT	I	Low	Power failure process completion flag (L : Complete, H : Normaly)
30	P13	×	I		For AGC Reading
31	P12	KEY02, MENU	I	Low	Front key input
32	P11	KEY01, OK	I	Low	Front key input
33	P10	KEY00, ←	I	Low	Front key input
43	INTP0	REM	I	High	Remote control input
44	INTP1	AC_CLK	I	Toggle	Power failuer detection clock (Both edge detectin)
45	P02	LNB_POW0	O	Any	LNB inernal / external (H : internal, L : external)
46	P03	LNB_POW1	O	Any	LNB 18V / 13V (H : 18V, L : 13V)
47	TI00	REM	I	High	Remote control input
48	P71	KEY, ↑	I		Front key input
49	P72	×	O		
50	P73	XSTBY	O	Low	Stand-by signal (H output at full power)
51	P74	KEY, ↓	I		Front key input
52	P75	KEY, →	I		Front key input
53	P64	XRESET_OMEGA	O	Low	STi5512 Reset
54	P65	RESET_CHDEC	O/I	High	Link IC Reset
55	P66	×	O		
56	P67	×	O		
57	P40	×	O		
58	P41	×	O		
59	P42	×	O		
60	P43	×	O		
61	P44	LED03	O	Low	Front LED, dig
62	P45	LED02	O	Low	Front LED, dig
63	P46	LED01	O	Low	Front LED, dig
64	P47	LED00	O	Low	Front LED, dig

8. PANEL FACILITIES AND SPECIFICATIONS

8.1 PANEL FACILITIES


Several functions keys
Movement on the display
Selection of program
Volume
Display of program number or time when terminal is in standby state
CANAL+ CANALSATELLITE
Reader for a bank debit card
Validation of settings
Power switch
Reader for a subscriber contract card
Access to PERSO screen


Connection of power cord (Cord provided to terminal)
Telephone line connection jack
PERITEL TV terminal (PERITEL TV : Application technology such as playback and recording video and TV games other than TV programs)
Input terminal for satellite antenna
SECTEUR 230V ~
SERIE
MODEM
PARALLELE
GAUCHE
DROITE
AUDIO HI-FI
PERITEL MAGNETOSCOPE
ENTREE ANTENNE
SORTIE ANTENNE
Series and parallel (option) computer connection terminal
Audio output terminal for connecting a stereo system
PERITEL video terminal
Parabola antenna output terminal for an analog satellite broadcast receiver

8.2 SPECIFICATIONS

RF

Moduration Method ..... QPSK
Symbol Rate 22, 27, 27.5Mbaud
Inner Code Rate 1/2, 2/3, 3/4, 5/6
Error Correction ..... Viterbi+Reed–solomon
Frequency Range ..... 950 to 2150MHz
Input Level ..... –65 to –25dBm
Max. Input Level 0dBm
Return Loss ..... 8.0dB min.
Spurious Signal and
Local Oscillator Level ..... –63dBm max.
LNB Power Supply ..... Ver. : 12.5V to 14V
Hor. : 17V to 19V

VIDEO

S/N ..... 55dB min.
Responce Flatness ..... –2 ± 2.5dB at 4.7MHz
Differential Gain ..... 10% max.
Differential Phase ..... 5deg max.
Chroma Delay ..... ±40nsec max.
Non Linearity ..... 5% max.

AUDIO

S/N ..... 72dB min.
Responce flatness ..... ±0.5dB at 20 to 20kHz
Channel Separation ..... 50dB min.

DATA COMMUNICATION

Serial Interface RS-232C
Parallel Interface IEEE1284
Modem V23
IC Card ISO-7816

GENERAL

Power Requirement AC230V/50Hz
Power Consumption ..... 18W typ.
Dimensions ..... 380 (W) X 253 (D) X 71 (H)
Net Weight 2.3kg